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(54) Solder ball connections and assembly process.

(57) High melting temperature Pb/Sn 95/5 solder balls (18) are connected to copper pads on the bottom of a ceramic chip carrier substrate (10) by low melting temperature eutectic Pb/Sn solder. The connection is made by quick reflow to prevent dissolving Pb into the eutectic solder and raising its melting temperature. Then the module is placed on a fiberglass-epoxy circuit board with the solder balls on eutectic Pb/Sn solder bumps on copper pads of the board. The structure is reflowed to simultaneously melt the solder on both sides of the balls to allow each ball to center between the carrier pad and circuit board pad to form a more symmetric joint. This process results in structure that are more reliable under high temperature cycling. Also, to further improve reliability, the balls are made as large as the I/O spacing allows without bridging beam on balls; the two pads are about the same size with more solder on the smaller pad; the pads are at least 75% of the ball diameter; and the eutectic joints are made as large as possible without bridging between pads. For reliability at even higher temperature cycles or larger substrate sizes columns are used instead of balls.

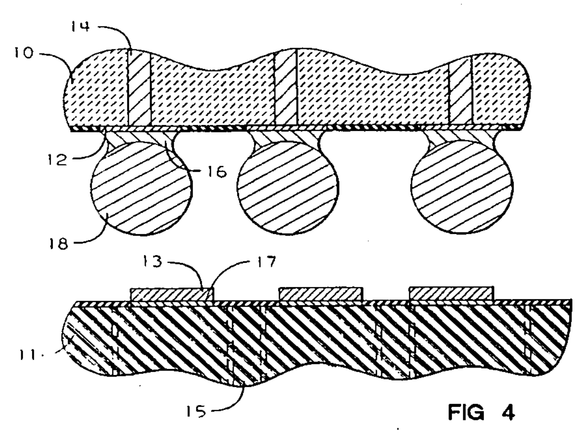

FIG 4

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FIELD OF THIS INVENTION

This invention relates to surface mount solder connections using HMT (high melting temperature) metal-balls between a grid of contacts on a component and a mirror image array of contacts of an electrical interconnect structure and more specifically to the composition of the HMT solder balls and LMT (low melting temperature) solder joining the balls to the contacts, the specific geometry of the connections, FR-4 (glass and epoxy) circuit boards and MLC (multi-layer ceramic) chip carriers for such interconnections, the processes for producing the boards and carriers, and the process for attaching the carriers to the boards.

BACKGROUND OF THIS INVENTION

Solder-ball connections have been used for mounting ICs (integrated computer chips) using the C-4 (controlled collapse chip connection) technology since first described in U.S. patents 3,401,126 and 3,429,040 by Miller. Packaging Electronic Systems by Dally (McGraw-Hill 1990 p. 113) describes flip chip or C-4 connections. In Dally, "Chip bond pads are deployed in an area array over the surface of the chip. ... These bonding pads are 5 mil in diameter on 10 mil centers. Matching bonding pads are produced on a ceramic substrate so that the pads on the chip and the ceramic coincide. Spheres of solder 5 mil in diameter are placed on the ceramic substrate pads ... and the chip is positioned and aligned relative to the substrate. The assembly is heated until the solder spheres begin to soften and a controlled collapse of the sphere takes place as the solder simultaneously wets both pads. A myriad of solder structures have been proposed for mounting IC chips as well as for interconnection to other levels of circuitry and electronic packaging."

"Ball Grid Arrays: The Hot New Package" by Terry Costlow and "Solder Balls Make Connections" by Glenda Derman both in Electronic Engineering Times March 15, 1993, describe using solder balls to connect ceramic or flexible chip carriers to circuit boards.

U. S. patent 4,132,341 to Bratschum describes the self-centering action of conductors spanning between solder pads of two components when both pads are simultaneously reflowed. U.S. patent 4,831,724 describes the self-centering of a component when it is vibrated during reflow.

Fabrication of multi-layer ceramic chip carriers is described in U.S. patents 3,518,756; 3,988,405; and 4,202,007 as well as "A Fabrication Technique For Multi-Layer Ceramic Modules" by H.D. Kaiser et al., Solid State Technology, May 1972, pp. 35-40 and "The Third Dimension in Thick-Films Multilayer Technology" by W. L. Clough, Microelectronics, Vol. 13, No. 9 (1970), pp. 23-30.

Fabrication of multi-layer circuit boards is described in U.S. patents 3,554,877; 3,791,858; and 3,554,877. Thin film techniques are described in U.S. patent 3,791,858.

U.S. patent 4,604,644 to Beckham describes materials and structures for encapsulating C-4 connections. U.S. patents 4,701,482 to Itoh and 4,999,699 to Christie et al. disclose epoxies and guidance in selecting epoxies for electronic applications.

Flexible film chip carriers (known in the art as ATAB) are described in U.S. patents 4,681,654; 4,766,670 and 5,159,535. In ATAB (area tape automated bonding) a flexible circuit board chip carrier is mounted on a circuit board using solder-ball connect.

U.S. patent 5,147,084 to Behun, describes using a HMP (high melting point) solder ball in association with a LMP (low melting point) solder. FIG 1A of that patent is similar to FIG 4 of this application. "A part 10 is to be joined to a board 11. Part 10 has internal metallurgy 14 which terminates at the surface at a bonding pads 12. A ... LMP solder 16 is applied to a bonding pad 12. A ... HMP solder ball 18 is placed in contact with LMP solder 16 and the assembly is heated to reflow the LMP solder which then wets to the non-molten HMP solder ball. ... Board 11 is also illustrated with internal metallurgy 15, terminating on the surface bonding pad 17. ... the assembled part 10 ... is brought into contact with part 11 having pad 17 and LMP solder 13, and the two are heated to a temperature sufficient to reflow the LMP solder but not sufficient to melt the HMP solder ball. The LMP solder 13 which is attached to the bonding pad 17, on board 11, will wet the HMP ball and connection will be achieved."

All the above sources are hereby incorporated by reference.

OBJECTS OF THIS INVENTION

Therefore, it is an object of this invention to provide a process for manufacturing a reliable interconnect assembly using ball connection.

More specifically, it is an object to connect two rigid, confronting substrates using HMT solder-ball connections to form an electronic packaging structure.

It is another object of this invention to provide a method of reflow soldering to produce solder-ball connections.

It is another object of this invention to provide methods for producing a component for solder-ball connection.

It is another object of this invention to provide methods of positioning solder-balls on such a component and reflow joining solder balls to the component for use in solder ball connection.

It is another object of this invention to provide a method of selecting HMT solder-ball size, selecting contact size, and selecting LMT solder volume.

It another object of this invention to provide a method of producing metal contacts on substrates for solder-ball connection.

Furthermore, it is an object of this invention to provide a reliable interconnect assembly in which HMT metal-balls are connected between mirror image arrays of contacts of two rigid, confronting substrates.

It is more specifically an object of this invention to define reliable LMT solder joint configurations between the balls and contacts.

It is another object of this invention to define ball sizes and contact sizes required for reliable connection.

It is another object of this invention to define HMT ball materials and LMT solder materials which permit reliable connections to be made.

It is another object of this invention to define substrates which may be used for reliable HMT solder-ball connection.

It is another object of this invention to define structures in a surface wiring layer of a substrate to connect between PTHs (plated through-holes) and connection pads for controlling LMT solder volumes for the joints between the pads and HMT solder-balls.

Finally, it is an object of this invention to describe an information handling system using the connections of the system.

SUMMARY OF THIS INVENTION

In this invention of applicants, it was discovered that solder-ball connections between confronting metal contact grids on rigid substrates which were made using a process similar to that which was used for ATAB were not reliable due to thermal fatigue of the solder joints between the balls and the contacts. It was discovered that the joints were not all symmetrical due to mis-registration of contacts (allowable tolerances in contact location) causing misalignment between confronting contacts, and that the joints could be made more symmetrical and more reliable by simultaneously reflowing the top and bottom LMT solder joints between each HMP metal-ball and both respective contacts of the ball. This allows the balls to be moved by surface tension of the melted solder to more symmetrical positions between the centers of the contacts within the plane defined by the array of the solder balls.

It was discovered that making the balls larger reduces fatigue, but that the size of the balls is constrained by the specified interconnection spacing and a nominal spacing between balls necessary to reliably prevent electrical connection from developing between the balls. Similarly, it was discovered that making the contacts larger reduces fatigue, but the size of the contacts are constrained by the specified interconnect spacing and the nominal spacing between contacts necessary to reliably prevent electrical connection from developing between contacts (e.g. solder bridging). For reliable interconnections fatigue is minimized by making the balls slightly smaller than the spacing between contacts and making the contacts slightly smaller than the balls. It was discovered that the reliability of the connections were affected by the relative size between the contacts on either side of each ball and that fatigue could be minimized by making the contacts equal sized. It was discovered that fatigue could be minimized, for different sized contacts on each side of the ball, by making the solder volume larger for the joint with the smaller contact.

It was discovered that increasing the cross section of the solder joints reduced fatigue but the volume increase is constrained by the necessity to reliably prevent solder bridging from developing between adjacent balls and between adjacent contacts. Finally it was discovered that reducing the cross section of the solder joints below about 2/3 of the diameter of the ball has a remarkably deleterious effect on the fatigue life of the connection.

The invention of applicants includes a process for producing an interconnect structure, comprising the steps of:

producing a rigid substrate with an approximately planer matrix of multiple, metal contacts on a major surface;

depositing a volume of a joining-material on each of the contacts of the matrix of the rigid substrate;

positioning a conductive metal-ball on the joining-material on each of the contacts on the first substrate to define a plane of metal-balls for maintaining a predetermined distance between the substrate and a second substrate to which the substrate is to be connected;

melting the volumes of joining-material without melting the metal-balls to prevent changing the shape of the balls; and

cooling the joining-material to form a solid mechanical joint between the metal-balls and the contacts of the first substrate.

The process for producing an interconnect structure, in which there is a metal element which can migrate between the metal-balls and the joining-material and increase the melting temperature of the joining-material and the step of melting is

performed at a minimum temperature and for a minimum time required to produce reliable joints for minimizing migration of metal elements between the metal-balls and first joining-material to minimize the increase of the melting temperature of the joining-material.

The process for producing an interconnect structure, further including the steps of:
selecting the size of the metal-balls slightly smaller than the spacing between the balls to maximize the size of the balls to minimize fatigue in the joints; and
selecting the size of the contacts:
slightly smaller than the size of the metal-balls as required to prevent joining-material from bridging between contacts; and
for confronting contacts, approximately equal in size to minimize fatigue in the joints.

The process for producing an interconnect structure, further including the steps of:
selecting ceramic for the material of the rigid substrate;
selecting copper for the material of the contacts; and
selecting a LMT (low melting temperature) solder alloy as the joining-material and a HMT (high melting temperature) solder for the metal-balls.

The process for producing an interconnect structure, further including the step of selecting re-enforced epoxy for the material of the rigid substrate.

The process for producing an interconnect structure, in which the step of producing a rigid substrate includes the steps of:
producing multiple green sheets of glass/ceramic particles and an organic binder;
making via holes in the sheets;
screen printing conductive material into the holes and onto one of the surfaces of the sheets to form a conductive pattern including the array of round contacts;
pressing the sheets together into a stack;
sintering the stack of sheets in an oven to form a multi-layer ceramic chip carrier with an array of copper contacts on a major surface which are about 0.7 mm in diameter, and are spaced about 1.25 mm apart;
selecting eutectic (about 37/63 percent) Pb/Sn solder alloy for the joining-material;
selecting a material of about 90% to about 95% Pb solder alloy and a size of about 0.9 mm for the metal-balls.

The process for producing an interconnect structure, further including the step of depositing sticky flux onto the contacts before positioning the metal-balls onto the contacts for holding the balls in place.

The process of producing an interconnect structure, further including the step of selecting elongated balls for interconnecting, and reflowing while holding the horizontal axis of the balls approximately perpendicular to the major surface of the substrate.

The process of producing an interconnect structure, further including the step of selecting elongated balls for interconnecting, and reflowing with the substrate horizontal inverted during reflow for gravity to hold the longitudinal axis of the balls vertically aligned.

The invention further includes, a process for fabricating an interconnect structure, comprising the steps of:
producing a fiberglass re-enforced epoxy board;
drilling one or more holes through the board;
plating the interior of the through-holes with conductive metal;
forming lands of conductive metal around the holes on a major surface of the board;
forming a rectangular array or grid of multiple, circular, conductive, metal contacts which are larger than the lands and positioned so that four contacts define a square that surrounds each of the lands;
forming a conductor extending in a diagonal direction in relation to the square to one of the contacts between each respective land and one of the surrounding contacts.

The process for fabricating an interconnect structure, in which the steps of plating the holes, forming lands, forming contacts and forming a conductor are performed simultaneously in an additive photo-lithographic process.

The process for fabricating an interconnect structure, further comprising the step of depositing joining-material on the contacts.

The immediately preceding process for fabricating an interconnect structure with deposited joining-material, further comprising the step of connecting to the joining-material, a metal-ball with a melting temperature substantially above the melting temperature of the joining-material.

The immediately preceding process for fabricating an interconnect structure, further comprising the step of heating to melt the joining-material to reflow connect the balls onto the contacts and then cooling the joining-material to solidify it.

The invention also includes a process for making an interconnect assembly, comprising the steps of:
producing an FR-4 board with a multitude of wiring layers;
forming circular copper lands in a wiring layer on a major surface of the board;
making holes through the lands and through the

board;
selectively depositing copper after drilling to plate the through-holes for connecting the lands to other wiring layers;
forming a rectangular array or grid of round copper contacts larger than the lands, about 0.7 mm diameter, and spaced at about 1.25 mm centers on the major surface and arranged so that four contacts define a square that surrounds each of the lands;
forming a conductor which is narrower than the contacts and narrower than the lands which extend between each of the lands surrounded by contacts in a diagonal direction in relation to the square of surrounding contacts;
depositing solder resist at least partially covering the conductor and the lands and extending between the contacts to prevent solder bridging;
depositing a joining solder material containing about 37/63% Pb/Sn solder alloy on each of the contacts in the array on the board;
producing multiple green sheets of glass/ceramic particles and an organic binder;
forming via holes through the sheets;
screen printing conductive material into the holes and onto one of the surfaces of the sheets to form a conductive pattern;
stacking the sheets together;
sintering the stack of sheets in an oven to form a multi-layer ceramic chip carrier with an array of copper contacts on a major surface which are about 0.7 mm wide, are spaced about 1.25 mm apart, and are arranged approximately mirror image to the array of contacts of the board;
forming an array of round contacts on an exterior major surface of the carrier;
depositing solder resist between the contacts to prevent solder bridging;
depositing a joining solder material containing about 37/63% Pb/Sn solder alloy on each of the contacts in the array on the carrier;
positioning a ball of about 90/10% Pb/Sn solder alloy and about 0.9 mm diameter in contact with the joining solder on each respective contact in the array of the carrier to define a plane of solder-balls;
reflowing to melt the joining solder material deposited on the contacts of the carrier without melting the solder-balls in order to solder the balls to the contacts of the carrier and using the minimal temperature and time required to form reliable mechanical joints in order to minimize diffusion of Pb from the balls into the melted solder;
cooling the carrier to solidify the joining solder;
positioning the ceramic carrier parallel to the circuit board with the solder-balls about in contact with the joining solder deposited on the array of contacts on the board so that each solder-ball is between a pair of contacts;
heating the substrates while positioned together to a temperature at which the solder deposited on the contacts of both the carrier and board are simultaneously melted and the solder-balls remain solid for moving the solder-balls by surface tension of the melted solder material in directions within the plane of the solder-balls to positions about midway between the centers of the pairs of contacts to produce symmetric connections between the substrates; and
cooling the substrates below the melting temperature of the solder materials to solidify the solder material.

The process for making an interconnect assembly, in which:
each of the contacts on the board include a very thin extension over the solder resist;
the solder is deposited on the contacts of the board, including the extensions, by wave soldering; and
the holes are formed in the board by drilling and formed in the sheets by punching;
and the process further comprises the steps of:
reflowing the deposited joining solder on the carrier before positioning the solder balls;
flattening the joining solder on the carrier before positioning the solder-balls on the carrier;
depositing sticky flux on the flattened joining solder on the carrier before positioning the solder-balls on the carrier;
reflowing the deposited solder on the board before positioning the carrier with the board;
flattening the joining solder on the board before positioning the carrier with the board; and
applying flux to the flattened joining solder for joining the balls to the board before positioning the carrier with the board.

The invention also includes an interconnect assembly comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on a major surface of each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a ball of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts; and
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the joining-materials of both the first and second volumes substantially less than the melting temperature of the metal-balls, with the first and second volumes of each pair of contacts connected to approximately diametrically opposite

ends of a respective metal-ball, and with the smallest cross sectional area of each joining-material volume having a minimum diameter at least about 2/3 of the diameter of the metal-ball.

The interconnect assembly, in which the balls are elongate with their longitudinal axis about perpendicular to the majro surface of each substrate.

The interconnect assembly, in which the diameter of the metal-balls and width of the contacts are about 0.6 mm to about 1.2 mm and the minimum diameter of such cross section of each joining-material volume is at least about 0.6 mm.

The immediately preceding interconnect assembly, in which the contacts are round with a diameter of about 0.7 mm and the diameter of the metal-balls is about 0.9 mm.

The interconnect assembly, in which the alloy of the metal-ball includes about 80% to about 97% Pb with most of the balance being Sn.

The immediately preceding interconnect assembly, in which the alloy of the metal-ball is from about 90% to about 95% Pb.

The interconnect assembly, in which the alloy of the joining-materials include approximately eutectic solder alloy.

The interconnect assembly, in which at least one of the substrates is multi-layer, and the structure further comprises one or more vias connecting between a surface wiring layer of the multi-layer substrate and another wiring layer of the multi-layer substrate which are integral with the contacts of a multi-layer substrate.

The interconnect assembly, in which the first and second joining-materials have about the same melting temperatures.

The interconnect assembly, in which a multitude of the contacts are connected with plated through-holes and in which the structure further comprises means to control the solder volume.

The interconnect assembly, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the first interconnect substrate further includes:
multiple wiring layers including one on a major surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

The immediately proceding interconnect assembly, in which:
the surface wiring layer containing the contacts further includes lands surrounding the vias;
the conductors extend from the lands to the contacts; and
the via through-holes are internally plated with a layer of copper sufficiently thick to electrically connect between the lands and other wiring layers of the structure.

The invention also includes a fabricated interconnect assembly comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a ball of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts; and
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the first and second joining-materials both substantially less than the melting temperature of the metal-balls, with the volumes of the first and second joining-materials of each pair of contacts connected to approximately diametrically opposite ends of a respective metal-ball, and with the melting temperatures of the first and second joining-materials being about equal.

The fabricated interconnect structure, in which:
the alloy of the metal-ball is from about 85% to about 97% Pb and most of the balance being Sn; and
the joining-material includes about 37/63 percent Pb/Sn solder alloy.

The immediately preceding fabricated interconnect structure, in which the joining-material is about 65 to about 75 percent Pb.

The invention also includes an interconnect structure comprising:
a substrate;
a planer pattern of multiple, metal contacts for interconnecting the substrate, to another substrate with mirror image contacts;
a ball of conductive metal for each contact with a diameter about the same as the width of the contacts;
a volume of a joining-material connected between each respective contact and the respective metal-ball for that contact, with a melting temperature of the joining-material substantially less than the melting temperature of the metal-ball, and with the smallest cross-sectional area of the joining-material

volumes having a minimum diameter at least about 2/3 of the diameter of the metal-ball.

The interconnect structure, in which the diameter of the metal-ball and width of the contacts are about 0.6 mm to about 1.2 mm and the minimum diameter of such cross section of each joining-material volume is at least about 0.6 mm.

The immediately proceeding interconnect structure, in which the diameters of the contacts are from about 15 to about 30% smaller than the diameters of the balls.

The immediately proceeding interconnect structure, in which the diameter of the metal-ball is about .9 mm and width of the contacts are about 0.7 mm.

The interconnect structure, in which the alloy of the metal-ball includes about 80% to about 97% Pb with substantially all the balance being Sn.

The immediately proceeding interconnect structure, 4 in which the alloy of the metal-ball is from 90% to 95% Pb.

The interconnect structure, in which the joining-materials include approximately eutectic solder alloy.

The interconnect structure, in which the joining-materials are about 25 to 50% Pb most of the balance being Sn.

The interconnect structure, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the substrate is a multi-layer ceramic substrate, and
the structure further comprises one or more vias connecting between a surface wiring layer of the multi-layer substrate and another wiring layer of the multi-layer substrate which are integral with the contacts of a multi-layer substrate and filled with a conductive material with a melting point significantly higher than the melting point of the joining-material.

The interconnect structure, 1 in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the substrate is an FR-4 circuit board and the structure further includes:
multiple wiring layers including one on the surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

The invention also includes, a fabricated interconnect structure comprising:
a multi-layer substrate having a wiring layer on the surface of the substrate;
a multitude of metal contacts in a matrix at positions defined by intersections of a grid of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface wiring layer;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

The fabricated interconnect structure, further comprising, a layer of solder resist covering most of each surface conductor, and with openings for the contacts.

The fabricated interconnect structure, further comprising round lands surrounding and connected to the vias; and in which the contacts are round, the lands are smaller in diameter than the contacts, and the diagonal connectors are narrower than the diameters of both the contacts and the lands.

The fabricated interconnect structure, in which the contacts are about 0.6 mm to about 1.2 mm in diameter, the width of the diagonal conductors are less than about half the diameters of the contacts.

The fabricated interconnect structure, in which the vias are partially open.

The fabricated interconnect structure, in which the vias are filled with a LMT solder.

The fabricated interconnect structure, in which the vias are plated through holes.

The invention includes an information handling system comprising:
one or more central processing units connected in a network;
random access memory communicating through a bus with each central processor unit;
input/output means for communicating with computer peripherals;
a circuit board in communication with one or more of the central processing units, with a planer pattern of round, metal contacts having a diameter of about 0.6 mm to about 1.0 mm on a major surface;
a chip carrier for one or more chips with a planer pattern of multiple, metal contacts on a major surface which is approximately a mirror image of a planer pattern of contacts on the circuit board to provide confronting pairs of contacts for intercon-

nection between the carrier and the board and which are also about 0.5 mm to about 1.0 mm in width;
a metal-ball for each respective pair of such contacts with a diameter of about 0.6 mm to about 1.3 mm;
a volume of a first joining-material for each pair of contacts connected to a respective contact of the chip carrier and a volume of a second joining-material for each pair of contacts connected to a respective contact of the circuit board, with melting temperatures of both the first and second joining-material substantially less than the melting temperature of the metal-balls, with the first and second joining-materials of each pair of contacts soldered to diametrically opposite ends of the respective metal-ball.

The information handling system of claim in which each joining-material volume has a cross section of at least 2/3 the diameter of the metal ball.

The information handling system, in which each joining-material volume has a cross section of at least about 0.6 mm.

The information handling system, in which the melting temperatures of the first and second joining-materials are about equal.

The information handling system, in which the confronting pairs of contacts are of about equal diameters.

The information handling system, in which the volumes of joining-material for the respective contacts are about inversely proportional to the diameters of the contacts.

The information handling system, in which the diameter of the contacts are about 15 to 30% smaller than the diameter of the metal-balls.

The information handling system, further comprising:
a layer of solder resist between the contacts of each of the patterns of contacts.

The information handling system, in which the circuit board is multi-layered and the contacts are associated with plated through holes and further comprising means to control the volume of the second joining-material.

The information handling system, in which:
the circuit board is multi-layered;
the positions of the contacts are defined by intersections of a multitude of approximately parallel equally spaced lines in each of two about perpendicular directions in a plane of the surfaces at the contacts; and
the circuit board further includes:
a multitude of wiring layers including one on the surface in which the contacts of the circuit board are positioned;
a multitude plated through holes connecting between one or more other wiring layers of the circuit board and the surface wiring layer for soldering to the metal-balls;
means to control the minimum diameter of the solder volume of soldered connections for the vias including:
a circular via land contact in the surface wiring layer for each respective via connected to the end of each via at the surface;
positioning the connections of the vias with the surface wiring layer at about the centers of squares defined by four of the contacts;
a metal conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via land and one of the four contacts surrounding the via land;
a covering of solder resist over the lands and conductors and which provides windows for the contacts.

The invention also includes interconnect apparatus comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a column of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts and positioned with a longitudinal axis perpendicular to the plane of contacts;
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the joining-materials of both the first and second volumes substantially less than the melting temperature of the metal-columns, with the first and second volumes of each pair of contacts connected to opposite ends of a respective metal-column.

The interconnect apparatus, in which the width of the contacts is about .5 to 1.2 mm and diameter of the metal-columns is less than or about equal to the width of the contacts.

The immediately proceeding interconnect apparatus, in which the contacts are round with a diameter of about .7 mm to .9 mm and the diameter of the metal-columns is about 0.1 mm to .3 mm less than the contacts.

The interconnect apparatus, in which the alloy of the metal-column includes about 80% to 97% Pb with most all the balance being Sn.

The immediately proceeding interconnect apparatus, in which the alloy of the metal-column is from 90% to 95% Pb.

The interconnect apparatus, in which the alloy of the joining-materials include approximately eutectic solder alloy.

The interconnect apparatus, in which each end of the columns are perpendicular to a longitudinal axis of the column.

The interconnect apparatus, in which the first and second joining-materials have about the same melting temperatures.

The interconnect apparatus, in which a multitude of the contacts are connected with plated through holes and in which the structure further comprises means to control the solder volume.

The interconnect apparatus, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the first interconnect substrate further includes:
multiple wiring layers including one on a major surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

The immediately proceeding interconnect apparatus, in which: the surface wiring layer containing the contacts further includes lands surrounding the vias;
the conductors extend from the lands to the conductors; and
the vias through holes which are internally plated with a layer of copper sufficiently thick to electrically connect between the lands and other wiring layers of the structure.

The invention also includes fabricated interconnect apparatus comprising:
a substrate;
a planer pattern of multiple, metal contacts for interconnecting the substrate, to another substrate with mirror image contacts;
a column of conductive metal for each contact with a diameter about the same as the width of the contacts and positioned about perpendicular to the plane of contacts;
a volume of a joining-material connected between each respective contact an the respective metal-column for that contact, with a melting temperatures of the joining-material substantially less than the melting temperature of the metal-column.

The fabricated interconnect apparatus, in which the width of the contacts is about 0.5 mm to about 1.2 mm and the metal columns are about .4 mm less to about .1 mm more than the width of the contacts.

The immediately proceeding fabricated interconnect apparatus, in which the width of the contacts is about .7 mm to about .9 mm and width of the metal column is about 0 to about .2 mm less than the width of the contacts.

The fabricated interconnect apparatus, in which the alloy of the metal-column includes about 80% to about 97% Pb with substantially all the balance being Sn.

The immediately proceeding fabricated interconnect apparatus, in which the alloy of the metal-column is from 90% to 95% Pb.

The fabricated interconnect apparatus, in which the joining-materials include approximately eutectic solder alloy.

The fabricated interconnect apparatus, in which the joining-materials are about 25 to 50% Pb most of the balance being Sn.

The fabricated interconnect apparatus, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the substrate is a multi-layer ceramic substrate, and
the structure further comprises one or more vias connecting between a surface wiring layer of the multi-layer substrate and another wiring layer of the multi-layer substrate which are integral with the contacts of a multi-layer substrate and filled with a conductive material with a melting point significantly higher than the melting point of the joining-material.

The fabricated interconnect apparatus, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the substrate is an FR-4 circuit board and the structure further includes:
multiple wiring layers including one on the surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of

the four contacts surrounding the via.

The invention also includes a process for interconnect assembly comprising the steps of:
producing a first substrate with an approximately planer pattern of multiple, metal contacts on a major surface;
depositing a volume of a first joining-material on each of the contacts of the first substrate;
connecting a conductive metal-column to the first joining-material on each of the contacts on the first substrate for maintaining a predetermined distance between the first substrate and a second substrate when connected;
producing a second substrate with a major surface having an approximately planer pattern of multiple, metal contacts which are approximately a mirror image of the pattern of contacts of the first substrate;
depositing a volume of a second joining-material for positioning between the metal-columns and each respective contact of the second substrate;
positioning the substrates together for interconnection with contact patterns parallel, with mirror image pairs of contacts in confronting approximate alignment, and with each volume of the second joining-material approximately in contact with a respective end of the metal-column and a respective contact of the second substrate;
simultaneously melting the first and second joining-materials while the substrates are positioned together, at a temperature in which the metal-columns remain solid for providing the predetermined separation between substrates, for moving the ends of the metal-columns by surface tension of the melted joining-material to positions approximately centers of the contacts;
cooling the substrates below the melting temperatures of the joining-materials to form electrical interconnections between the pairs of contacts.

The process for interconnect assembly, in which the volumes of the second joining-material are deposited on the contacts of the second substrate prior to positioning the substrates together for interconnection.

The process for interconnect assembly, in which the volumes of second joining-material are deposited at projecting ends of the metal-columns after the columns are connected to the first substrate prior to positioning the substrates together for interconnection.

The process for interconnect assembly, in which the step of connecting a metal-column to the first volumes of joining-material includes the steps of:
positioning a metal-column on each volume of first joining-material;
heating the first substrate up to connect the metal-columns to the contacts of the first substrate by melting the first joining-material without melting the metal-columns; and
cooling the first substrate down to form a mechanical joint between the metal-columns and the contacts of the first substrate before the step of positioning the substrates together for interconnection.

The immediately proceeding process for interconnect assembly, in which there is a metal element which can migrate between the metal-columns and the first joining-material and increase the melting temperature of the first joining-material and during the step of heating the first substrate up the substrate is heated to a minimum temperature and for a minimum time for minimizing migration of a metal elements between the metal-columns and first joining-material to minimize the increase of the melting temperature of the first joining-material.

The immediately proceeding process for interconnect assembly, further comprising the step, selecting a different joining-material for the first and second joining-materials for compensating for migration of the metal element between the metal-columns and first joining-material in order for the first and second joining-materials to simultaneously melt during the step of heating the substrates up while positioned together.

The process for interconnect assembly, in which there is a metal element which can migrate between the metal-columns and the joining-materials and which increases the melting temperature of the joining-materials, and the substrates are heated together at a sufficiently high temperature for a sufficiently long time to allow migration of the metal element between the metal-columns and joining-materials to substantially raise the melting temperature of the joining-materials so that the interconnections connections are not remelted during subsequent joining of attachments to the substrates using substantially the same joining-material as the volumes of joining-material.

The process for interconnect assembly, further including the steps of:
selecting the size of the contacts as large as possible while reliably preventing joining-material bridging between contacts; and
selecting the size of the metal-columns the same size or slightly smaller than the spacing between the contacts to maximize the size of the columns while reliably preventing solder-bridging and to minimize fatigue in the columns.

The process for interconnect assembly, further including the steps of:
depositing a liquid encapsulating material between the substrates around the metal-columns in the area defined by the contact pattern after the step of cooling the substrates below joining-material melting temperatures; and
hardening the encapsulating material to reduce the

stresses in the joints during subsequent thermal cycling of the connected substrates.

The process for interconnect assembly, further comprising the steps of:
selecting a shape for the contacts to maximize the size of the contacts which may be reliably connected without bridging for making the size of the contacts larger to reduce thermal fatigue; and
depositing solder resist between the contacts for making the size of the contacts which may be reliably connected without bridging larger to reduce thermal fatigue.

Finally the invention includes a process for building an interconnect structure comprising the steps of:
making a rigid substrate with an approximately planer matrix of multiple, metal contacts on a major surface;
depositing a volume of a joining-material on each of the contacts of the matrix of the rigid substrate;
positioning a conductive metal-column to the joining-material on each of the contacts on the first substrate for maintaining a predetermined distance between the substrate and a second substrate to which the substrate is to be connected;
melting the volumes of joining-material without melting the metal-columns to prevent changing the shape of the columns; and
cooling the joining-material to form a solid mechanical joint between the metal-columns and the contacts of the substrate.

The process for building an interconnect structure, in which there is a metal element which can migrate between the metal-columns and the joining-material and increase the melting temperature of the joining-material and during the step of melting is performed at a minimum temperature and for a minimum time required to produce reliable joints for minimizing migration of a metal elements between the metal-columns and first joining-material to minimize the increase of the melting temperature of the joining-material.

The process for building an interconnect structure, further including the steps of:
selecting the size of the contacts as large as possible limited only by reliably preventing joining-material bridging between contacts; and
selecting the size of the metal-columns about the same size or slightly smaller than the contacts to maximize the size of the columns to minimize fatigue in the joints without causing solder bridging.

The process for building an interconnect structure, further including the steps of:
selecting ceramic for the material of the rigid substrate;
selecting copper for the material of the contacts; and
selecting a LMT (low melting temperature) solder alloy as the joining-material and a HMT (high melting temperature) solder for the metal-columns.

The process for building an interconnect structure, further including the step of selecting FR-4 for the material of the rigid substrate.

The process for building an interconnect structure, in which the step of making a rigid substrate includes the steps of:
producing multiple green sheets of glass/ceramic particles and an organic binder;
making via holes in the sheets;
screen printing conductive material into the holes and onto one of the surfaces of the sheets to form a conductive pattern including the array of round contacts;
pressing the sheets together into a stack; and
sintering the stack of sheets in an oven to form a multi-layer ceramic chip carrier with an array of copper contacts on a major surface which are about .7 mm in diameter, are spaced about 1.25 mm apart;
selecting eutectic (about 63/37) Pb/Sn solder alloy for the joining-material;
selecting a material of 90 to 95% Pb solder alloy and a size of about .9 mm for the metal-columns.

The process for building an interconnect structure, further including the step of depositing sticky flux onto the contacts before positioning the metal-columns onto the contacts for holding the columns in place.

The process for building an interconnect structure, further including the step of holding the column vertical during reflow to join the column to the module.

The process for building an interconnect structure, further including the step of inverting the module during reflow to join the columns to the module.

This invention will be described in greater detail in reference to the following drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a process diagram which illustrates producing an multi-layer ceramic chip carrier (MLC) of this invention.

FIG. 2 illustrates the process for producing an fiberglass-epoxy circuit board (FR-4) of this invention.

FIG. 3 illustrate the process for producing the connections between the MLC and FR-4 in this invention.

FIG. 4 is a schematic partial cross section of a specific embodiment of this invention showing part of an MLC chip carrier with solder balls attached to contacts and confronting mirror image contacts of an FR-4 circuit board.

FIG. 5 shows the positioning of solder balls on the solder contacts prior to attachment to the MLC of FIG. 4.

FIG. 6 shows the MLC and FR-4 of FIG. 4 positioned together.

FIG. 7 shows the reflow connections of the MLC to the FR-4 of FIG. 4 in which only the joint between the solder balls and the FR-4 is melted during reflow.

FIG. 8 illustrates the reflow connections of the MLC to the FR-4 of FIG. 4 in which both joints of each connection are simultaneously melted to provide a more symmetric connection.

FIG. 9 is a schematic cross section through line 9-9 of FIG. 10, illustrating the "dog bone" connection between plated-through-hole via connection of this invention.

FIG. 10 is a schematic plan view illustrating part of the array of metal contacts and "dog bone" connections between the plated through holes and contacts.

FIG. 11 is larger view of the "dog-bone" arrangement of FIG. 10.

FIG. 12 is another embodiment of this invention with different sized contacts and inversely proportional solder volumes.

FIG. 13 is a plan view of a contact of this invention for providing sufficient solder volumes for this invention.

FIG. 14 is a cross section of the contact of FIG. 13 through line 14-14.

FIG. 15 schematically illustrates the information handling system of this invention.

DESCRIPTION OF EMBODIMENTS INCLUDING THE BEST MODE

In this invention, as illustrated in FIG 4, a first substrate 10 is produced with a planer array of contacts 12 and vias 14. In this application substrate refers to any component with a flat surface for interconnection which will be referred to as a major surface in contrast to a thin edge surface. Although the invention will increase the reliability of connecting flexible circuit boards such as ATAB (area tape automated bonding) components, preferably the first substrate is a component such as an FR-4, plastic, or ceramic chip carrier, and more preferably a MLC (multi-layer ceramic) chip carrier for which this inventions of this application are especially well suited.

As illustrated in FIG. 1, step 101, in the manufacture of ceramic chip carriers, ceramic powders are mixed with binders, solvents and plasticizer and cast to form green sheets to form dielectric layers. In step 102, Vias are made preferably by punching and in step 103, conductive ink or paste (e.g. Mo frit and solvent) is screened to fill the vias. The wiring pattern may also be screened on the surface at this time and/or exterior wiring layers may be made later using a thin film process. For multi-layer ceramic, in step 104, green sheets are stacked and laminated with heat and pressure into a monolithic structure. Then the green sheet(s) are sintered, in step 105, by firing in an oven with a reducing atmosphere. After sintering the exposed metal is coated for protection (not shown). A thin film process may be used to produce an exterior wiring layer (not shown). For example, conductive metal may be evaporated or sputtered onto the substrate followed by photolithographic patterning which may be followed by dialectic coating and additional thin film layering.

The contacts 12 (FIG. 4) may be square or more preferably are approximately round to match the shape of the ball and to allow a closer spacing sufficient to reliably prevent solder bridging. The contacts may be made from any conductive substance, preferably a metal such as Al or Ti and more preferably are made from or covered with Cu, Ni, Au, Pd, or alloys of these. The material may be deposited by screening or a photolithographic process may be followed by chemical and/or electric deposition processes.

In step 106 (FIG. 1), the contacts 12 are covered with a volume of a first joining-material 13, 16 respectively, such as a conductive thermoplastic or a solder alloy containing Sn, Pb, Bi, In, Ag to form solder contacts or solder bumps. In the preferred embodiment the joining-material is Pb/Sn solder with 20 to 75 % Sn and the balance mostly Pb and most preferably is about eutectic 63% Sn and 37% Pb. The solder may be deposited in the molten state by a mass soldering method such as wave soldering or may be screened as solder paste (metal particles in a organic carrier) or may be electrically and/or chemically deposited on the contacts following a photolithographic process.

In step 107, as shown in FIG. 5, metal-balls are attached to the solder bumps preferably by applying a layer of sticky flux 20 on which the balls are positioned. The balls may be placed simultaneously by transfer from a vacuum die. The flux may be applied just on the contacts or in the entire area of the substrate interconnections. The balls 18 may be copper preferably coated to prevent oxidation, or more preferably are a HMT solder alloy with a melting temperature substantially more than that of the joining-material so that the balls may be reflow joined to the contacts in step 108 without melting the balls. Preferably the balls are Sn and 80 to 97 % Pb most preferably 90 - 95 % Pb. Preferably the attachment is made reliable by reflow heating to join the ball to the contact so the ball will not fall off during later processing. During reflow of the first joining-material 16, surface tension of the melted

joining-material will precisely align balls 18 with contacts 12. Centering the balls on the pads of the first substrate helps align the balls with the pads of the second substrate.

For solder joining-materials, during reflow, metal elements will dissolve or be transported between the LMT solder and the metal-balls. In order to prevent this the reflow attachment of the balls 18 to substrate 10 should be done at the lowest temperature and in shortest time required to center the balls and prevent losing the balls during subsequent processing.

In step 109 the substrate is cooled to solidify the joining-material.

A second substrate 11 is produced which also has vias 15 and a planer array of contacts 17. The array of contacts 17 is approximately a mirror image of the array of contacts 12. The second substrate may be a flexible circuit board (e.g. thin polyimide and copper layers), or more preferably a rigid board such as ceramic and is most preferably a multi-layer FR-4 printed circuit board. This inventions of this application are especially well suited to applications where there is a significant difference in the thermal coefficients between rigid first and second substrates.

FIG. 2 illustrates the process of manufacturing fiberglass-epoxy circuit boards (FR-4). In step 120, one or more layers of fiberglass cloth are impregnated with epoxy resin solution to form a dielectric layer. For boards with multiple FR-4 layers the layers are only partially cured to form stable B-stage layers. In step 121, at least the internal layers are circuitized. FIG's 9 - 11 illustrate the surface wiring of this invention and is discussed in more detail later. This step includes forming a rectangular array of preferably round contacts forming lands for connection to the vias at the centers of squares defined by four surrounding contacts, and forming connections between the lands and contacts. Usually before drilling for vias that go through all the layers, the B-stage layers are laminated in step 122 with heat and pressure to fuse the layers and fully cure the board. Each layer is circuitized by screening or by a photolithographic process in which a metal foil covering is subtractively removed or metal is selectively chemically and/or electrically added to form a wiring layer on the surface of the layer. In step 123, holes are drilled at the lands, through one or more layers, and in step 124, the holes are internally plated with metal (preferably copper) to form vias for electrical interconnection between the wiring layers on each side of the dielectric layers.

In step 125 joining-material is deposited on contacts in a similar manner as previously described for step 106 in the process of producing MLC.

In step 131, substrates 10, 11 are moved into confronting position as shown in FIG. 4, and in step 132, are brought together as shown in FIG. 6. The accuracy of the placement machine is limited so that the substrates are not precisely aligned.

FIG. 7 shows the results of reflow of only joining-material 13 which moves substrate 10 in the direction of arrow 40 relative to substrate 11 into precise alignment between the substrates. As illustrated, the connections, such as on either side of ball 42, are not symmetric due to tolerances in the positions of the contacts. Therefore, in step 133, as shown in FIG. 8, preferably both joining-materials 13 and 16 on either side of the solder balls 18 are simultaneously reflowed to produce more symmetric connections. When both joints 51 and 52 are simultaneously melted the surface tension of the joining-material will move the ball in the plane 53 of the balls toward a position halfway between the centers 54, 55 of the contacts resulting in a more symmetric connection. Such symmetric connections have a greater fatigue life than the non-symmetric connections of FIG. 7.

In step 134, the substrates are cooled to solidify the joining-material of the connections. In step 135, the area between the first and second substrates around the metal-balls is filled with an encapsulant such as epoxy. It is critical to the solder connection configuration invention of applicant that the connections not be encapsulated until after simultaneous reflow of the top and bottom solder joints so that the solder balls can move into alignment between the contacts. After such alignment encapsulating the area between the substrates, around the balls, reduces fatigue stress during thermal cycling.

When Balls 18 is reflow attached to contacts 12, some material will be exchanged between the ball and joining-material 16. For example if the ball is 10/90 Sn/Pb and the joining-material is eutectic 63/37 Sn/Pb then after reflow the joining-material will have a higher Pb content and therefore a higher melting temperature. If joining-material 13 is also eutectic Sn/Pb solder then during reflow for connecting the substrates the joints are going to have to be heated to the higher temperature to simultaneously melt. In order to use a minimum temperature for reflow joining-material 16 may have a lead content reduced below eutectic amounts so that during the first reflow it becomes eutectic and then the simultaneous melting during the second reflow is achieved at minimum temperatures.

Most preferably the balls in FIG's 1-5 are as large as possible to minimize fatigue stress in the connections only limited by the requirement of reliably preventing bridging between the balls. Stresses in the joints on either side of the balls would be minimized by making the contacts the

same size as the balls, however, to reliably prevent bridging between the contacts, the contacts have to be significantly smaller than the balls. As shown in FIG. 8, preferably a solder mask material 53, 54 which repels liquid solder is placed between the contacts to reduce solder bridging so the contacts may be made as close to the size of the balls as possible. For example, connections with 9 mm balls and round contacts of 7 mm diameter spaced at 1.25 mm centers may be reliably made without bridging.

/* what are some typical solder mask materials */

Solder volumes should be as large as possible to reduce fatigue but are limited by the requirement to reliably prevent bridging and the cost or difficulty of depositing large volumes of solder. Most preferably, as shown in FIG. 9, in plane 62 defined as the cross section of minimum diameter of the joint 64, the diameter is at least 2/3 of the diameter of the ball 66. For example if the ball is 9 mm in diameter, the joint should be at least 6 mm in diameter in plane 62 and more preferably larger.

For ceramic substrates through hole vias are usually filled with a HMP metal, and for thin film layers on ceramic, flex, or FR-4, vias are usually filled or are slightly depressed in relation with contacts that are not on vias. For multi-layer flexible and FR-4 substrates, wiring layers usually contain round lands of metal through which the via holes are formed and which are interconnected between wiring layers by plating the hole. Some of the contacts on FR-4 and flex substrates may occur on such plated vias. Since the diameter of the solder joint is critical, the volume of solder is critical, but the volume can not easily be controlled at such holes (even if previously filled with solder).

FIG. 10 schematically shows an arrangement of plated through hole vias 71 each connected to a solder contact 72. This "dog bone" arrangement prevents the solder on contact 72 from flowing into the through hole 73. In this specific embodiment the centers of the contacts are about at the intersections of multiple equally spaced parallel lines 74 and multiple equally spaced parallel lines 75 which are perpendicular to lines 74. Vias 71 are located at the centers of squares 76 defined by four contacts 72 aground via 71. The vias are connected to the contacts through a wire 77 extending under a layer of solder mask 78.

FIG. 11 schematically illustrates a single "dog bone" 80 of this invention prior to depositing joining-material on contact 82. A hole 81 (hidden) is made by mechanical or laser drilling into the substrate at least to another wiring layer, and metal is deposited to form contact 82, land 83, connecting wire 84 and to plate the hole 85 leaving opening 86. Solder mask 87 covers most of connecting wire 87 and the outer edge of land 83 as indicated by dashed lines to prevent solder bridging.

FIG. 12 schematically illustrates an alternative embodiment in which metal contact 91 is larger than metal contact 92. In this case in order to reduce fatigue and increase fatigue life of the connection, a higher volume of joining-material 93 is placed between ball 94 and the smaller contact 92, than the volume of solder material 95 between the solder ball and larger contact 91. Thus the minimum cross sections of the joints on each side of the solder ball may be made about equal to equalize fatigue at each joint of the connection.

FIG's 13 and 14 illustrate a technique to provide higher levels of solder deposited on a contact than can usually be deposited by wave soldering or electrical or chemical (electroless) deposition. Flash layer 130 extends out from contact pad 132 over the layer of solder resist 134 the thickness of the flash is exaggerated for illustration. Solder 136 is deposited electrically, chemically, or preferably by solder wave. The flash is a conductive substance for electrical deposition, a seed materials such as palladium for electroless plating, and may be a solder wettable material for wave soldering. The flash material is selected to dissolve during reflow resulting in all the solder migrating onto the contact pad. Preferably for wave soldering the flash is copper of tin which is sufficiently thick to survive during deposition, but thin enough to fully dissolve during reflow. The thickness of the solder deposited by molten solder wave generally increases as the size of the flash area increases.

FIG. 15 shows an information handling system 150 in which computer assembly 151 includes central processor module 152 communicating through one or more wiring layers (not shown) in substrate 153 with computer memory module 154. Computer 152 communicates with computer assembly 155 through cable 156. Computer 155 also includes central processor module 152 communicating through one or more wiring layers (not shown) in substrate 158 with computer memory module 158. One or preferably both modules of each computer are connected to the substrate using the preferred solder ball or solder column connections of the invention.

FIG. 16 illustrate solder columns 160 which are similar to the solder balls 18 (FIG. 4) and the previous discussion on materials, geometries, and methods of placement, reflow joining to the modules, reflow connection to the substrates are applicable. They have approximately semi-circular ends and are preferably from 1 to 20 times longer then their diameters. Fatigue is reduced by making the columns longer, but longer columns result in higher module profiles, reduced lead cooling and

handling problems that militate against length exceeding that necessary to reliably prevent thermal fatigue failures. In this application the term solderball includes hemispherical ended solder columns. In order to join the columns to the module, columns may be reflow heated while attached to the bottom side of the module (i.e. inverted position). This results the columns being closely centered on the contacts and very accurately vertically aligned.

In FIG. 17, columns 171 have square ends formed for example from cutting extruded solder wire. Vacuum die 172 includes a flat face 173 with recesses which fit the solder ball or solder column. The recesses communicate with a vacuum reservoir 175 through passages 176 which are significantly smaller than the solder balls or columns to reliably prevent the columns from entering vacuum reservoir 175 and prevent jamming. The vacuum die is used to position the balls or columns on the contacts of a substrate either as shown in FIG 17 or in an inverted position. Either round or square end columns can be reflow joined in inverted position as in FIG 16 or by holding the columns vertical during reflow preferably using the vacuum die. The vacuum can be turned off or even reversed during reflow allowing the columns to rest against the solder contacts.

When the round or square columns are held in position during reflow joining with the contacts of substrate 178, the columns are not as well centered on the contacts, or as vertically aligned or vertically positioned as the joints formed by hanging. As shown in FIG. 18 when the module substrate is connected to another substrate 181 the joints are not symmetrical. When the simultaneous reflow of the invention is applied as shown in FIG. 19, the joints become much more symmetrical and more reliable.

While this invention has been described in relation to preferred embodiments, it will be understood by those skilled in the art that changes in the details of processes and structures may be made without departing from the spirit and scope of this invention.

Claims

1. A process for producing an interconnect assembly comprising the steps of:
producing a first substrate with an approximately planer pattern of multiple, metal contacts on a major surface;
depositing a volume of a first joining-material on each of the contacts of the first substrate;
connecting a conductive metal-ball to the first joining-material on each of the contacts on the first substrate to define a plane of metal-balls for maintaining a predetermined distance between the first substrate and a second substrate when connected;
producing a second substrate with a major surface having an approximately planer pattern of multiple, metal contacts which are approximately a mirror image of the pattern of contacts of the first substrate;
depositing a volume of a second joining-material for positioning between the metal-balls and each respective contact of the second substrate;
positioning the substrates together for interconnection with contact patterns parallel, with mirror image pairs of contacts in confronting approximate alignment, and with each volume of the second joining-material approximately in contact with a respective metal-ball and a respective contact of the second substrate;
simultaneously melting the first and second joining-materials while the substrates are positioned together, at a temperature in which the metal-balls remain solid for providing the predetermined separation between substrates, for moving the metal-balls by surface tension of the melted joining-material in directions within the plane of the joining metal-balls to positions approximately between the pairs of approximately aligned contacts;
cooling the substrates below the melting temperatures of the joining-materials to form electrical interconnections between the pairs of contacts.

2. The process of claim 1, in which the step of connecting a metal-ball to the first volumes of joining-material includes the steps of:
positioning a metal-ball on each volume of first joining-material;
heating the first substrate up to connect the metal-balls to the contacts of the first substrate by melting the first joining-material without melting the metal-balls; and
cooling the first substrate down to form a mechanical joint between the metal-balls and the contacts of the first substrate before the step of positioning the substrates together for interconnection.

3. The process of claim 1, in which the step of connecting a metal-ball to the first volumes of joining-material includes the steps of:
positioning a metal-ball on each volume of first joining-material;
heating the first substrate up to connect the metal-balls to the contacts of the first substrate by melting the first joining-material without melting the metal-balls; and
cooling the first substrate down to form a me-

chanical joint between the metal-balls and the contacts of the first substrate before the step of positioning the substrates together for interconnection.

4. The process of claim 3, in which there is a metal element which can migrate between the metal-balls and the first joining-material and increase the melting temperature of the first joining-material and during the step of heating the first substrate up the substrate is heated to a minimum temperature and for a minimum time for minimizing migration of a metal elements between the metal-balls and first joining-material to minimize the increase of the melting temperature of the first joining-material.

5. The process of claim 4, further comprising the step, selecting a different joining-material for the first and second joining-materials for compensating for migration of the metal element between the metal-balls and first joining-material in order for the first and second joining-materials to simultaneously melt during the step of heating the substrates up while positioned together.

6. A process for forming an interconnect assembly comprising the steps of:
producing a first substrate having on a major surface, a wiring layer including an array of multiple, metal contacts;
producing a second substrate having on a major surface, a wiring layer including an array of multiple, metal contacts which are arranged approximately mirror image to the contacts of the first substrate and are about the same size as the contacts of the first substrate;
positioning the substrates with the mirror image arrays of contacts in confrontation to define confronting pairs of contacts;
positioning conductive metal-balls between the pairs of confronting contacts;
connecting joining-material between the metal-balls and each of the respective pair of contacts to electrically and mechanically interconnect the pairs of contacts through the balls.

7. A process for building an interconnect assembly comprising the steps of:
producing a first substrate having on a major surface, a wiring layer including an array of multiple, metal contacts;
producing a second substrate having on a major surface, a wiring layer including an array of multiple, metal contacts which are arranged approximately mirror image to the contacts of the first substrate and are larger in size than the contacts of the first substrate;
positioning the substrates with the mirror image arrays of contacts in confrontation to define confronting pairs of contacts;
positioning conductive metal-balls between the pairs of confronting contacts;
connecting a volume of joining-material between the metal-balls and the respective contact of the first substrate;
connecting a smaller volume of joining-material between the metal-balls and the respective contact of the second substrate to electrically and mechanically interconnect the pairs of contacts.

8. A process for producing an interconnect structure comprising the steps of:
producing a rigid substrate with an approximately planer matrix of multiple, metal contacts on a major surface;
depositing a volume of a joining-material on each of the contacts of the matrix of the rigid substrate;
positioning a conductive metal-ball to the joining-material on each of the contacts on the first substrate to define a plane of metal-balls for maintaining a predetermined distance between the substrate and a second substrate to which the substrate is to be connected;
melting the volumes of joining-material without melting the metal-balls to prevent changing the shape of the balls; and
cooling the joining-material to form a solid mechanical joint between the metal-balls and the contacts of the substrate.

9. A process for fabricating an interconnect structure comprising the steps of:
producing a FR-4 board;
drilling through the board;
plating the through holes with conductive metal;
forming lands of conductive metal around the holes on a major surface of the board;
forming a rectangular array or grid of multiple, circular, conductive, metal contacts which are larger than the lands and positioned so that four contacts define a square that surrounds one or more of the lands;
forming a conductor extending in a diagonal direction in relation to the square to one of the contacts between each respective land and one of the surrounding contacts.

10. The process of claim 1, further comprising the step of depositing joining-material on the contacts.

11. The process of claim 10, further comprising the step of connecting to the joining-material, a metal-ball with a melting temperature substantially above the melting temperature of the joining-material.

12. The process of claim 11, further comprising the step of heating to melt the joining-material to reflow connect the balls onto the contacts and then cooling the joining-material to solidify it.

13. A process for making an interconnect assembly comprising the steps of:
producing an FR-4 board with a multitude of wiring layers;
forming circular copper lands in a wiring layer on a major surface of the board;
making holes through the board through the lands;
selectively depositing copper after drilling for platting the through holes for connecting the lands to other wiring layers;
forming a rectangular array or grid of round copper contacts larger than the lands about .7 mm diameter and spaced at about 1.25 mm centers and positioned so that four contacts define a square that surrounds each of the lands;
forming a conductor which is narrower than the contacts and narrower than the lands which extending between each of the lands surrounded by contacts in a diagonal direction in relation to the square of surrounding contacts;
depositing solder resist at least partially covering the conductor and the lands and extending between the contacts to prevent solder bridging;
depositing a joining solder material containing about 63/37 Pb/Sn solder alloy on each of the contacts in the array on the board;
producing multiple green sheets of glass/ceramic particles and an organic binder;
forming via holes through the sheets;
screen printing conductive material into the holes and onto one of the surfaces of the sheets to form a conductive pattern;
stacking the sheets together;
sintering the stack of sheets in an oven to form a multi-layer ceramic chip carrier with an array of copper contacts on a major surface which are about .7 mm wide, are spaced about 1.25 mm apart, and are arranged approximately mirror image to the array of contacts of the board;
forming an array of round contacts on exterior major surface of the carrier;
depositing solder resist between the contacts to prevent solder bridging;
depositing a joining solder material containing about 63/37 Pb/Sn solder alloy on each of the contacts in the array on the carrier;
positioning a ball of about 90/10 Pb/Sn solder alloy and about .9 mm diameter in contact with the joining solder material deposited on each respective contact in the array of the carrier to define a plane of solder balls;
reflowing to melt the joining solder material deposited on the contacts of the carrier without melting the solder balls in order to solder the balls to the contacts of the carrier and using the minimal temperature and time required to form reliable mechanical joints in order to minimize diffusion of Pb from the balls into the melted solder;
cooling the carrier to solidify the joining solder;
positioning the ceramic carrier parallel to the circuit board with the solder balls about in contact with the joining solder deposited on the array of contacts on the board so that each solder ball is between a pair of contacts;
heating the substrates while positioned together to a temperature at which the solder deposited on the contacts of both the carrier and board are simultaneously melted and the solder-balls remain solid for moving the solder-balls by surface tension of the melted solder material in directions within the plane of the solder-balls to positions about midway between the centers of the pairs of contacts to produce symmetric connections between the substrates;
cooling the substrates below the melting temperature of the solder materials to solidify the solder material.

14. The process of claim 13, in which:
each of the contacts on the board include a very thin extension over the solder resist;
the solder is deposited on the contacts of the FR-4 board including the extensions by wave soldering; and
the holes are formed in the FR-4 board by drilling and formed in the sheets by punching;
and the process further comprises the steps of:
reflowing the deposited joining solder on the carrier before positioning the solder balls;
flattening the joining solder of the carrier before positioning the solder balls;
depositing sticky flux on the joining solder of the carrier before positioning the solder balls;
reflowing the deposited solder on the board before positioning the carrier with the board;
flattening the joining solder of the carrier before positioning the carrier with the board;

applying flux for joining the balls to the board before positioning the carrier with the board.

15. An interconnect assembly comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a ball of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts;
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the joining-materials of both the first and second volumes substantially less than the melting temperature of the metal-balls, with the first and second volumes of each pair of contacts connected to approximately diametrically opposite ends of a respective metal-ball, and with the smallest cross sectional area of each joining-material volume having a minimum diameter at least about 2/3 of the diameter of the metal-ball.

16. The structure of claim 15, in which the diameter of the metal-balls and width of the contacts are about 0.6 mm to about 1.2 mm and the minimum diameter of such cross section of each joining-material volume is at least about 0.6 mm.

17. The structure of claim 16, in which the contacts are round with a diameter of about .7 mm and the diameter of the metal-balls is about 0.9 mm.

18. The structure of claim 17, in which the alloy of the metal-ball includes about 80% to 97% Pb with most all the balance being Sn.

19. The structure of claim 18, in which the alloy of the metal-ball is from 90% to 95% Pb.

20. The structure of claim 15, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the first interconnect substrate further includes:
multiple wiring layers including one on a major surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

21. The structure of claim 20, in which:
the surface wiring layer containing the contacts further includes lands surrounding the vias;
the conductors extend from the lands to the conductors; and
the vias through holes which are internally plated with a layer of copper sufficiently thick to electrically connect between the lands and other wiring layers of the structure.

22. A fabricated interconnect assembly comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a ball of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts;
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the first and second joining-materials both substantially less than the melting temperature of the metal-balls, with the volumes of the first and second joining-materials of each pair of contacts connected to approximately diametrically opposite ends of a respective metal-ball, and with the melting temperatures of the first and second joining-materials being about equal.

23. The structure of claim 22, in which:
the alloy of the metal-ball is from 85% to 97% Pb and the balance of the material being Sn;
the joining-material includes about 63/37 percent Pb/Sn solder alloy.

24. The structure of claim 23, in which the joining-material is 65 to 75 percent Pb.

25. An interconnect structure comprising:
a substrate;
a planer pattern of multiple, metal contacts for interconnecting the substrate, to another substrate with mirror image contacts;
a ball of conductive metal for each contact with a diameter about the same as the width of the contacts;
a volume of a joining-material connected between each respective contact an the respective metal-ball for that contact, with a melting temperatures of the joining-material substantially less than the melting temperature of the metal-ball, and with the smallest cross sectional area of the joining-material volumes having a minimum diameter at least about 2/3 of the diameter of the metal-ball.

26. The structure of claim 1, in which the diameter of the metal-ball and width of the contacts are about 0.6 mm to about 1.2 mm and the minimum diameter of such cross section of each joining-material volume is at least about 0.6 mm.

27. The structure of claim 26, in which the diameters of the contacts are from about 15 to about 30% smaller than the diameters of the balls.

28. The structure of claim 27, in which the diameter of the metal-ball is about .9 mm and width of the contacts are about 0.7 mm.

29. The structure of claim 25, in which the alloy of the metal-ball includes about 80% to about 97% Pb with substantially all the balance being Sn.

30. The structure of claim 29, in which the alloy of the metal-ball is from 90% to 95% Pb.

31. A fabricated interconnect structure comprising:
a multi-layer substrate having a wiring layer on the surface of the substrate;
a multitude of metal contacts in a matrix at positions defined by intersections of a grid of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface wiring layer;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

32. An information handling system comprising:
one or more central processing units connected in a network;
random access memory communicating through a bus with each central processor unit;
input/output means for communicating with computer peripherals;
a circuit board in communication with one or more of the central processing units, with a planer pattern of round, metal contacts having a diameter of about 0.6 mm to about 1.0 mm on a major surface;
a chip carrier for one or more chips with a planer pattern of multiple, metal contacts on a major surface which is approximately a mirror image of a planer pattern of contacts on the circuit board to provide confronting pairs of contacts for interconnection between the carrier and the board and which are also about 0.5 mm to about 1.0 mm in width;
a metal-ball for each respective pair of such contacts with a diameter of about 0.6 mm to about 1.3 mm;
a volume of a first joining-material for each pair of contacts connected to a respective contact of the chip carrier and a volume of a second joining-material for each pair of contacts connected to a respective contact of the circuit board, with melting temperatures of both the first and second joining-material substantially less than the melting temperature of the metal-balls, with the first andsecond joining-materials of each pair of contacts soldered to diametrically opposite ends of the respective metal-ball.

33. The system of claim 32, in which:
the circuit board is multi-layered;
the positions of the contacts are defined by intersections of a multitude of approximately parallel equally spaced lines in each of two about perpendicular directions in a plane of the surfaces at the contacts; and
the circuit board further includes:
a multitude of wiring layers including one on the surface in which the contacts of the circuit board are positioned;
a multitude plated through holes connecting between one or more other wiring layers of the circuit board and the surface wiring layer for soldering to the metal-balls;
means to control the minimum diameter of the

solder volume of soldered connections for the vias including:
a circular via land contact in the surface wiring layer for each respective via connected to the end of each via at the surface;
positioning the connections of the vias with the surface wiring layer at about the centers of squares defined by four of the contacts;
a metal conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via land and one of the four contacts surrounding the via land;
a covering of solder resist over the lands and conductors and which provides windows for the contacts.

34. Information handling apparatus comprising:
one or more central processing units connected in a network;
random access memory communicating through a bus with each central processor unit;
input/output means for communicating with computer peripherals;
a multi-layer circuit board in communication with one or more of the central processing units, having a wiring layer on the surface of the circuit board;
a multitude of metal contacts in a planer matrix pattern at positions defined by intersections of a grid of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface wiring layer;
a multitude of conducting vias connecting between one or more other wiring layers of the circuit board and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via;
a chip carrier for one or more chips with a planer pattern of multiple, metal contacts on a major surface which is approximately a mirror image of a planer pattern of contacts on the circuit board to provide confronting pairs of contacts for interconnection between the carrier and the board;
a metal-ball for each respective pair of such contacts;
a volume of a first joining-material for each pair of contacts connected to a respective contact of the chip carrier and a volume of a second joining-material for each pair of contacts connected to a respective contact of the circuit board, with melting temperatures of both the first and second joining-material substantially less than the melting temperature of the metal-balls, with the first and second joining-materials of each pair of contacts soldered to diametrically opposite ends of the respective metal-ball.

35. Interconnect apparatus comprising:
a first and second interconnect substrates;
a planer pattern of multiple, metal contacts on each respective substrate, for interconnection between the substrates, which are mirror images of each other to provide confronting pairs of contacts;
a column of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts and positioned with a longitudinal axis perpendicular to the plane of contacts;
a volume of a first joining-material for each such pair of contacts connected to the respective contact of the first interconnect substrate and a volume of a second joining-material for each such pair of contacts connected to the respective contact of the second interconnect substrate, with melting temperatures of the joining-materials of both the first and second volumes substantially less than the melting temperature of the metal-columns, with the first and second volumes of each pair of contacts connected to opposite ends of a respective metal-column.

36. The structure of claim 35, in which:
the positions of the contacts are defined by intersections of a multitude of parallel equally spaced lines in each of two perpendicular directions in a plane of the surface at the contacts; and
the first interconnect substrate further includes:
multiple wiring layers including one on a major surface of the substrate in which the contacts are positioned;
a multitude of conducting vias connecting between one or more other wiring layers of the substrate and the surface wiring layer at about the centers of squares defined by four of the contacts;
a conductor of the surface wiring layer for each respective via, which is substantially narrower than the contacts, and extends in a diagonal direction of the square to connect between the via and one of the four contacts surrounding the via.

37. The structure of claim 36, in which:
the surface wiring layer containing the contacts

further includes lands surrounding the vias;
the conductors extend from the lands to the conductors; and
the vias through holes which are internally plated ith a layer of copper sufficiently thick to electrically connect between the lands and other wiring layers of the structure.

38. Fabricated interconnect apparatus comprising:
a substrate;
a planer pattern of multiple, metal contacts for interconnecting the substrate, to another substrate with mirror image contacts;
a column of conductive metal for each contact with a diameter about the same as the width of the contacts and positioned about perpendicular to the plane of contacts;
a volume of a joining-material connected between each respective contact an the respective metal-column for that contact, with a melting temperatures of the joining-material substantially less than the melting temperature of the metal-column.

39. The structure of claim 38, in which the alloy of the metal-column includes about 80% to about 97% Pb with substantially all the balance being Sn.

40. The structure of claim 39, in which the alloy of the metal-column is from 90% to 95% Pb.

41. A process for producing an interconnect assembly comprising the steps of:
producing a first substrate with an approximately planer pattern of multiple, metal contacts on a major surface;
depositing a volume of a first joining-material on each of the contacts of the first substrate;
connecting a conductive metal-column to the first joining-material on each of the contacts on the first substrate for maintaining a predetermined distance between the first substrate and a second substrate when connected;
producing a second substrate with a major surface having an approximately planer pattern of multiple, metal contacts which are approximately a mirror image of the pattern of contacts of the first substrate;
depositing a volume of a second joining-material for positioning between the metal-columns and each respective contact of the second substrate;
positioning the substrates together for interconnection with contact patterns parallel, with mirror image pairs of contacts in confronting approximate alignment, and with each volume of the second joining-material approximately in contact with a respective end of the metal-column and a respective contact of the second substrate;
simultaneously melting the first and second joining-materials while the substrates are positioned together, at a temperature in which the metal-columns remain solid for providing the predetermined separation between substrates, for moving the ends of the metal-columns by surface tension of the melted joining-material to positions approximately centers of the contacts;
cooling the substrates below the melting temperatures of the joining-materials to form electrical interconnections between the pairs of contacts.

42. The process of claim 41, in which the step of connecting a metal-column to the first volumes of joining-material includes the steps of:
positioning a metal-column on each volume of first joining-material;
heating the first substrate up to connect the metal-columns to the contacts of the first substrate by melting the first joining-material without melting the metal-columns; and
cooling the first substrate down to form a mechanical joint between the metal-columns and the contacts of the first substrate before the step of positioning the substrates together for interconnection.

43. The process of claim 42, in which there is a metal element which can migrate between the metal-columns and the first joining-material and increase the melting temperature of the first joining-material and during the step of heating the first substrate up the substrate is heated to a minimum temperature and for a minimum time for minimizing migration of a metal elements between the metal-columns and first joining-material to minimize the increase of the melting temperature of the first joining-material.

44. The process of claim 43, further comprising the step, selecting a different joining-material for the first and second joining-materials for compensating for migration of the metal element between the metal-columns and first joining-material in order for the first and second joining-materials to simultaneously melt during the step of heating the substrates up while positioned together.

45. A process for producing an interconnect structure comprising the steps of:
producing a rigid substrate with an approxi-

mately planer matrix of multiple, metal contacts on a major surface;
depositing a volume of a joining-material on each of the contacts of the matrix of the rigid substrate;
positioning a conductive metal-column to the joining-material on each of the contacts on the first substrate for maintaining a predetermined distance between the substrate and a second substrate to which the substrate is to be connected;
melting the volumes of joining-material without melting the metal-columns to prevent changing the shape of the columns; and
cooling the joining-material to form a solid mechanical joint between the metal-columns and the contacts of the substrate.

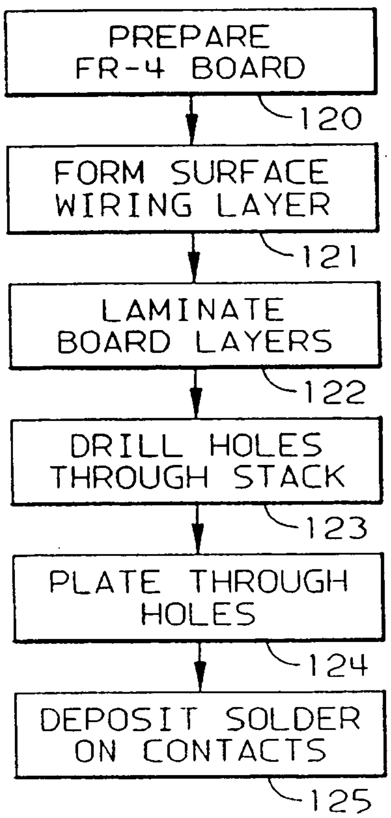


FIG. 2

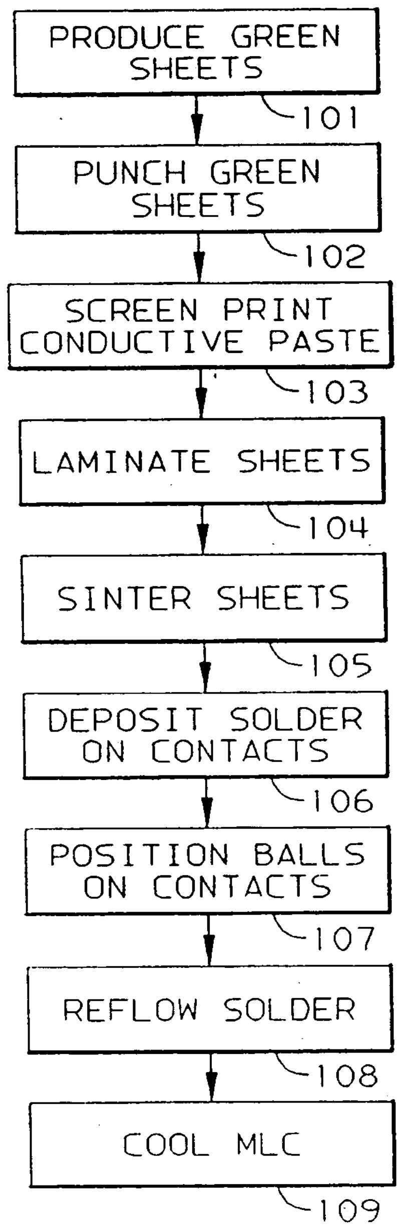


FIG. 1

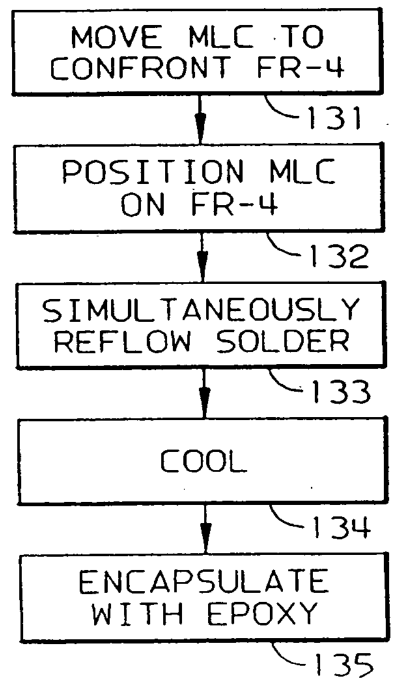


FIG. 3

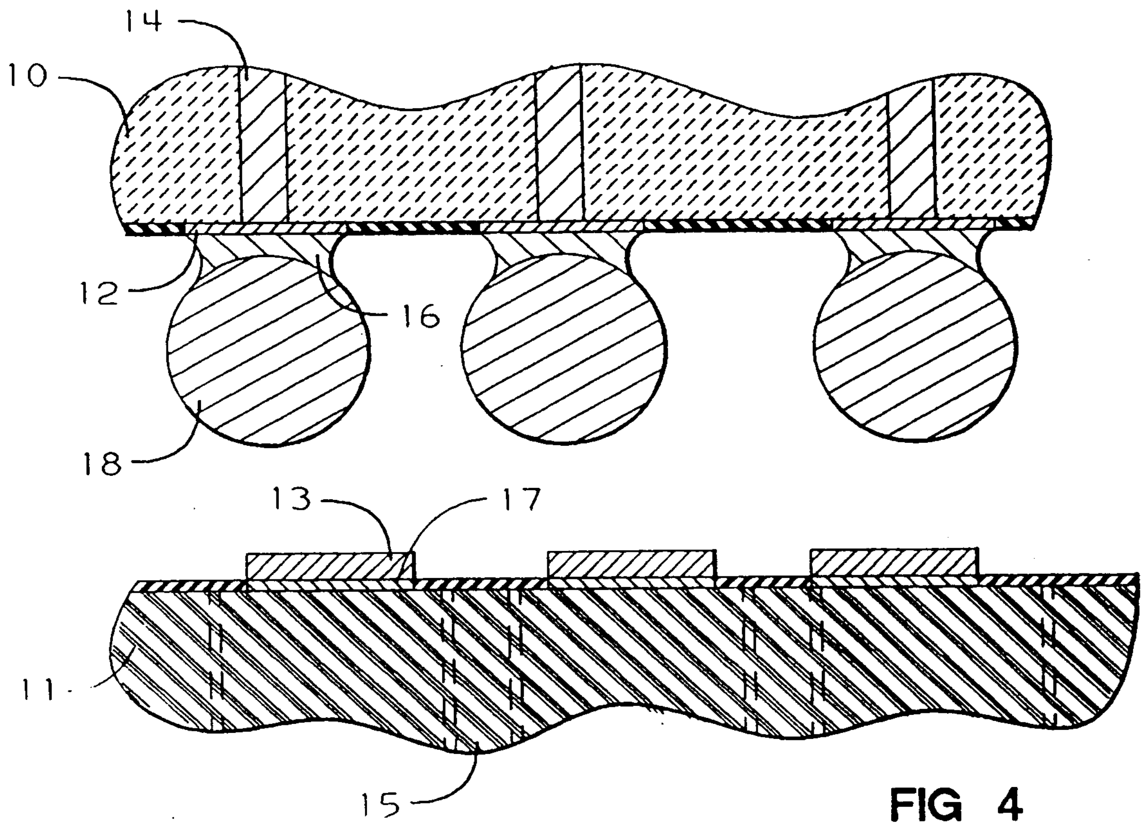


FIG 4

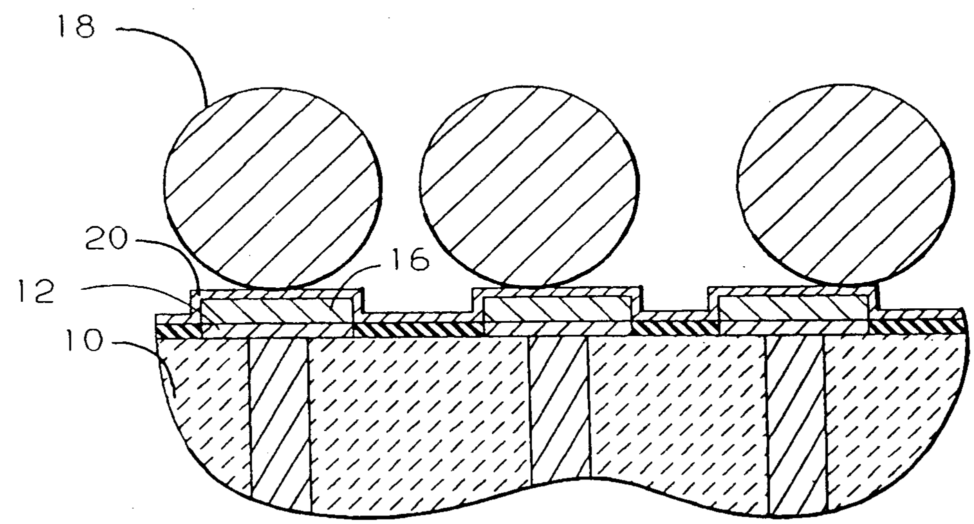


FIG 5

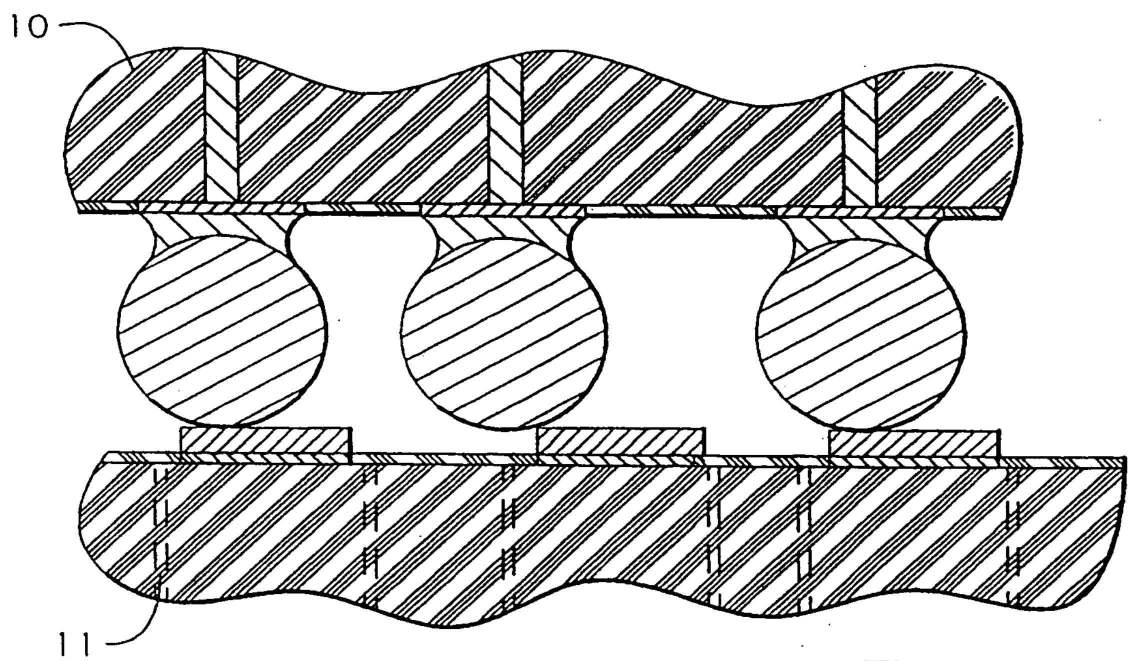


FIG. 6

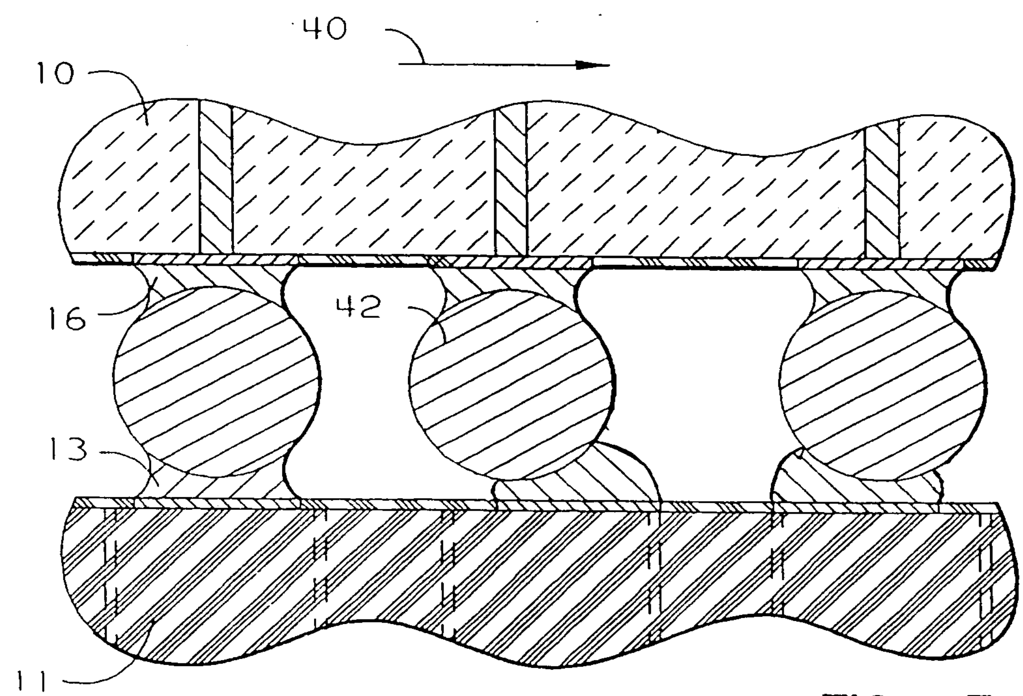


FIG. 7

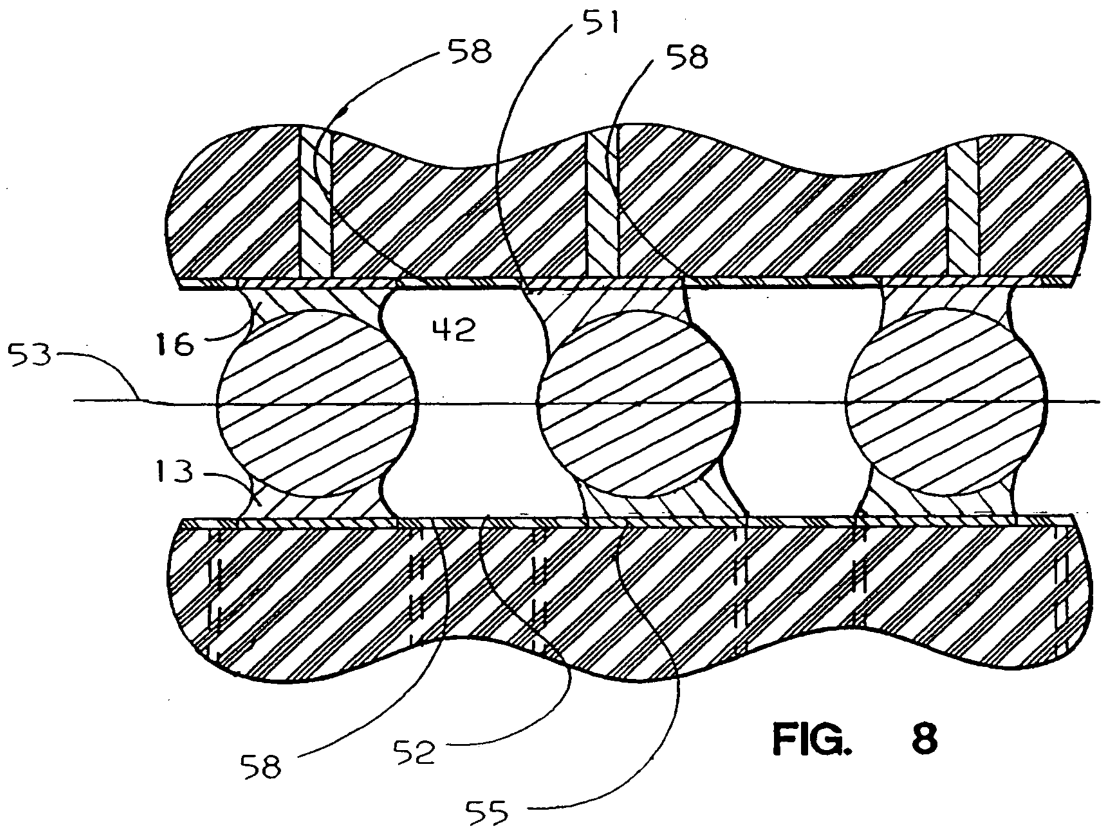


FIG. 8

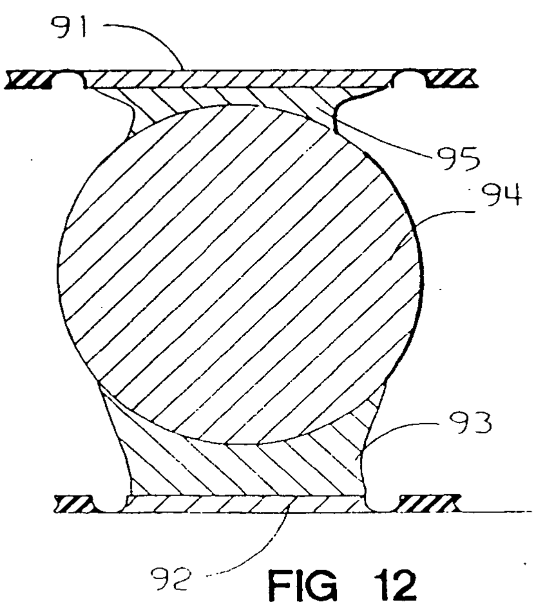


FIG 12

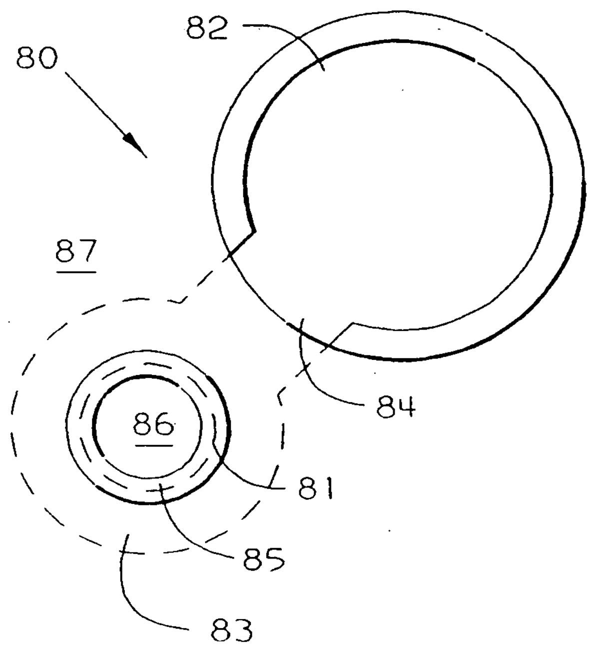
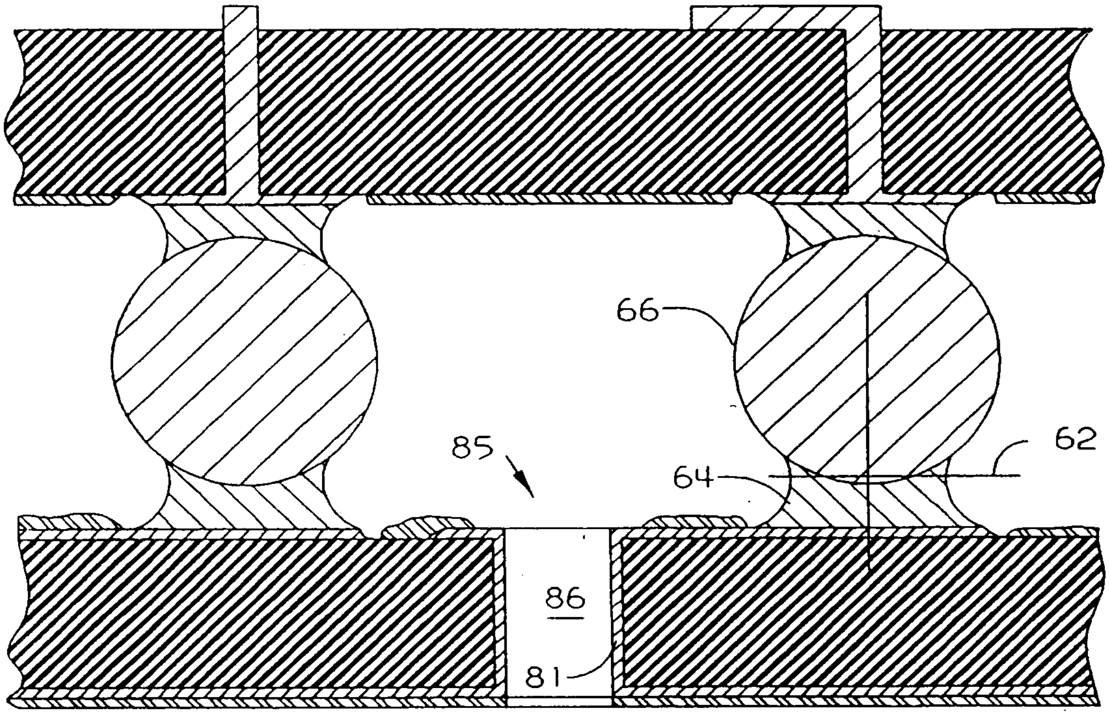


FIG. 11

FIG. 9



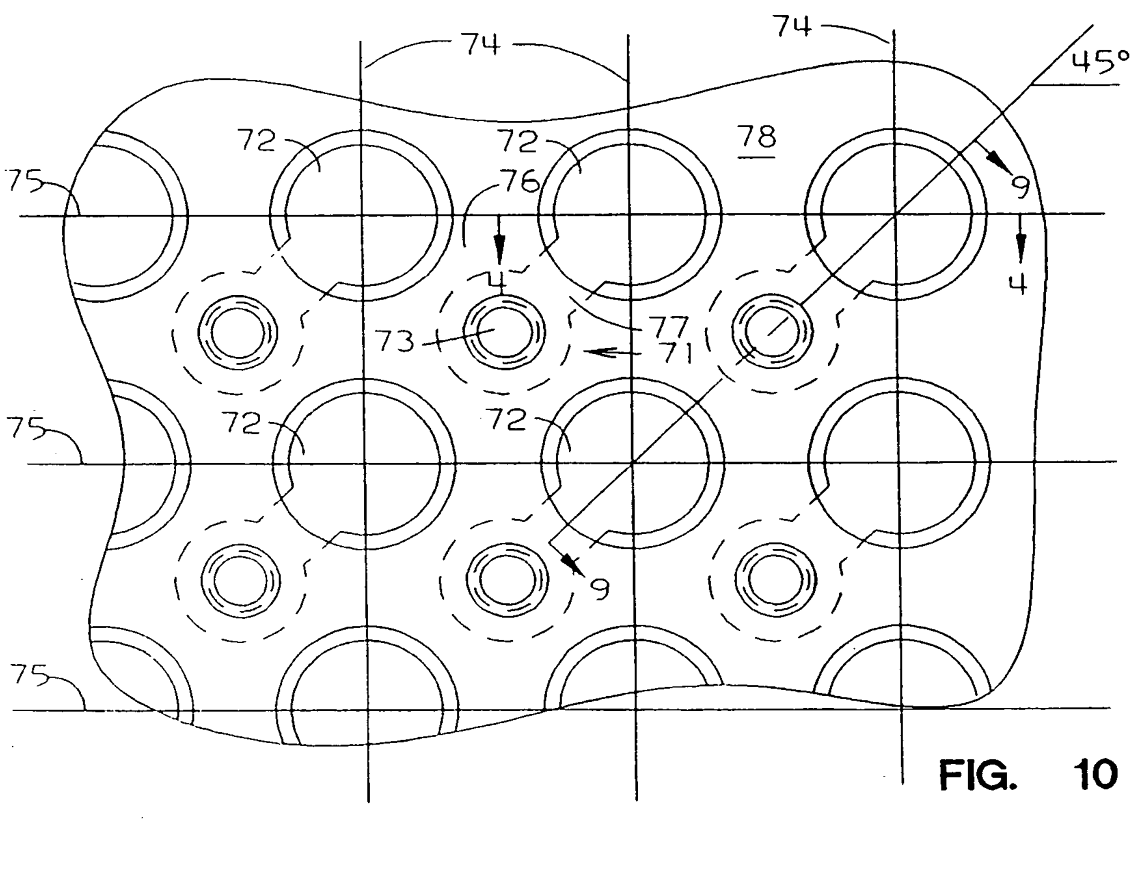


FIG. 10

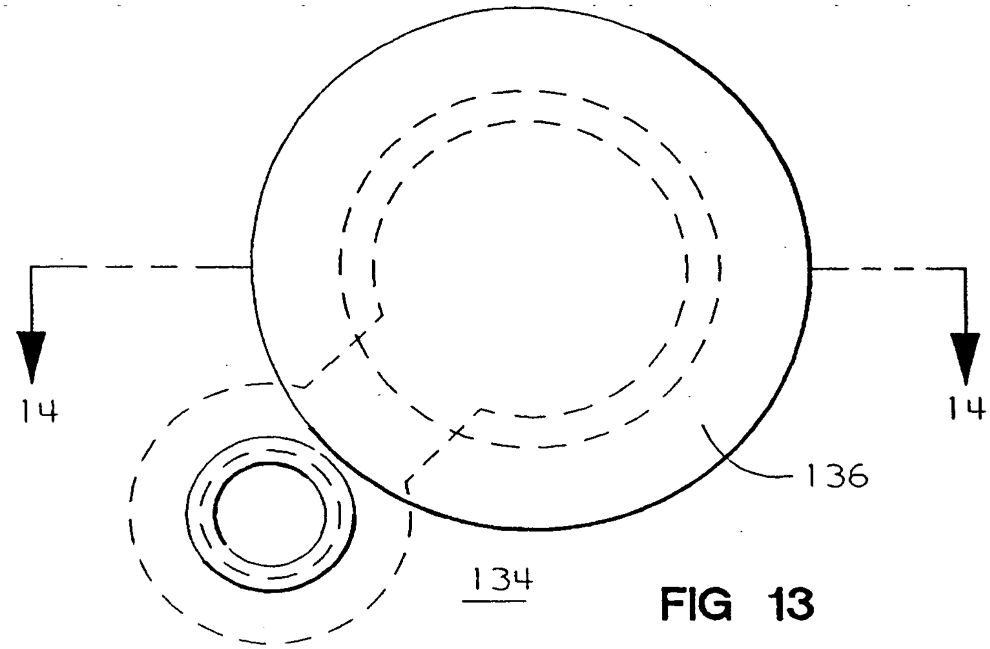


FIG 13

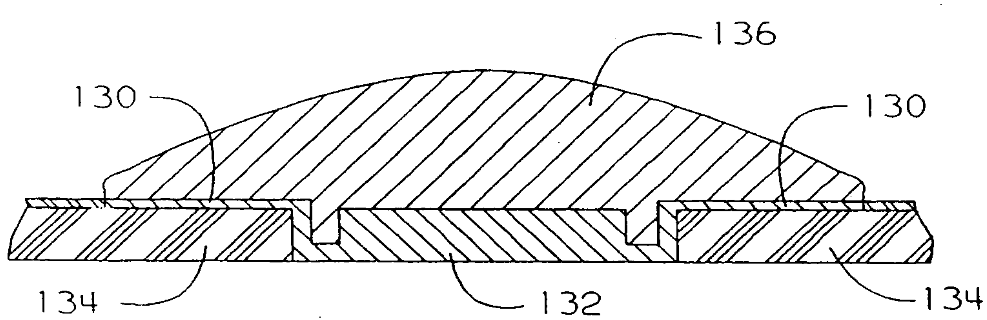


FIG 14

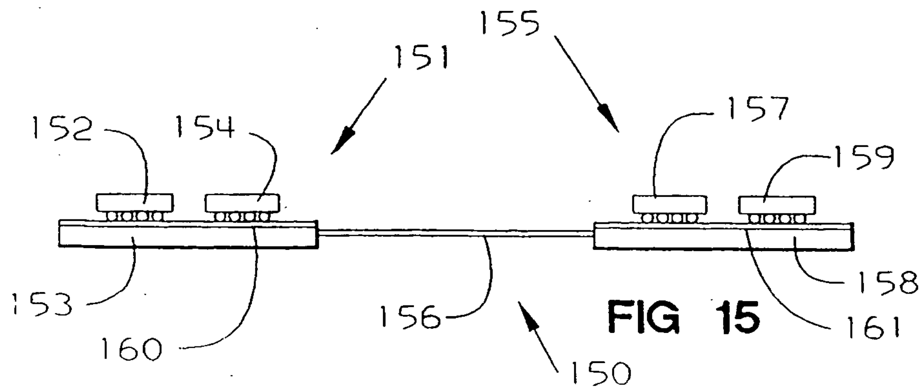


FIG 15

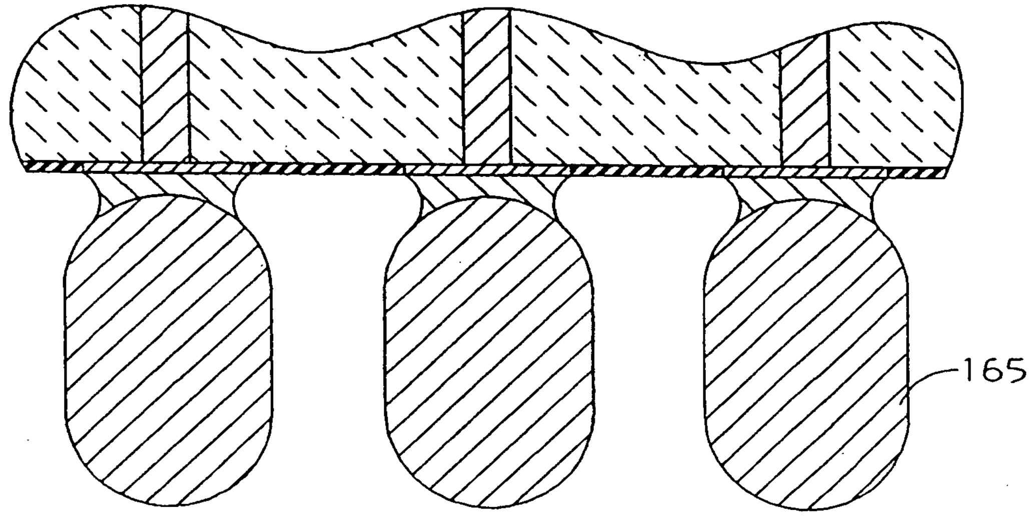


FIG 16

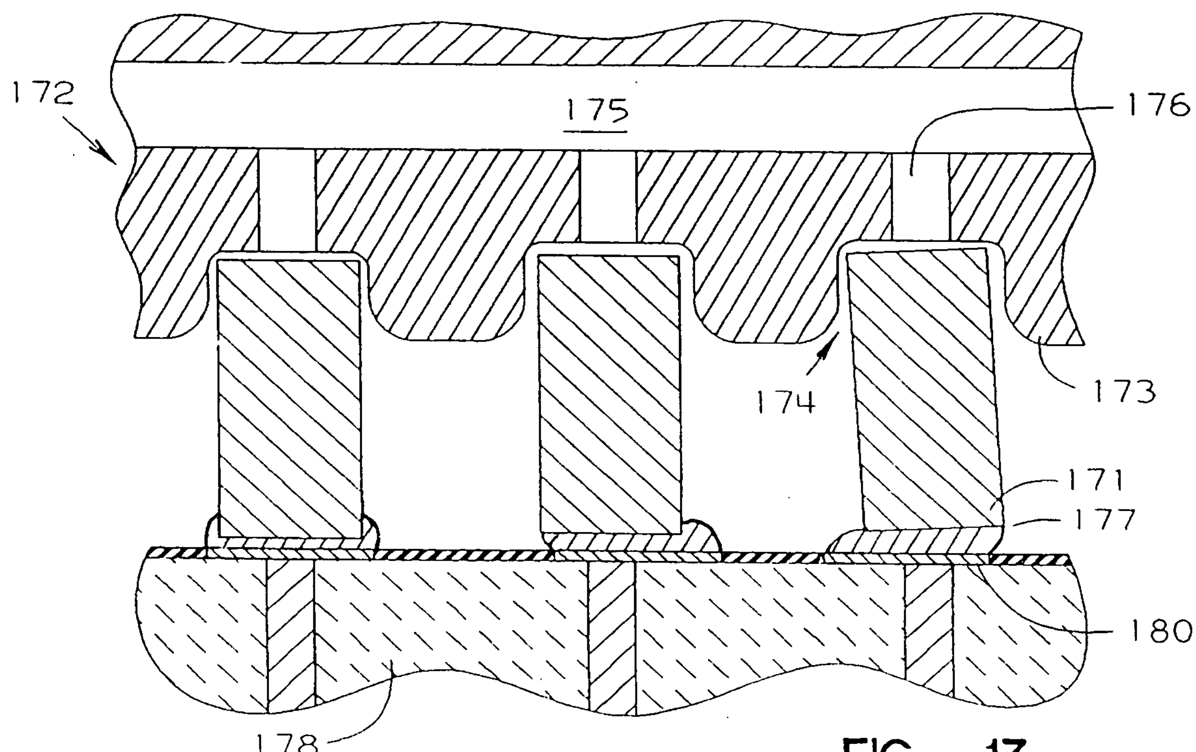


FIG. 17

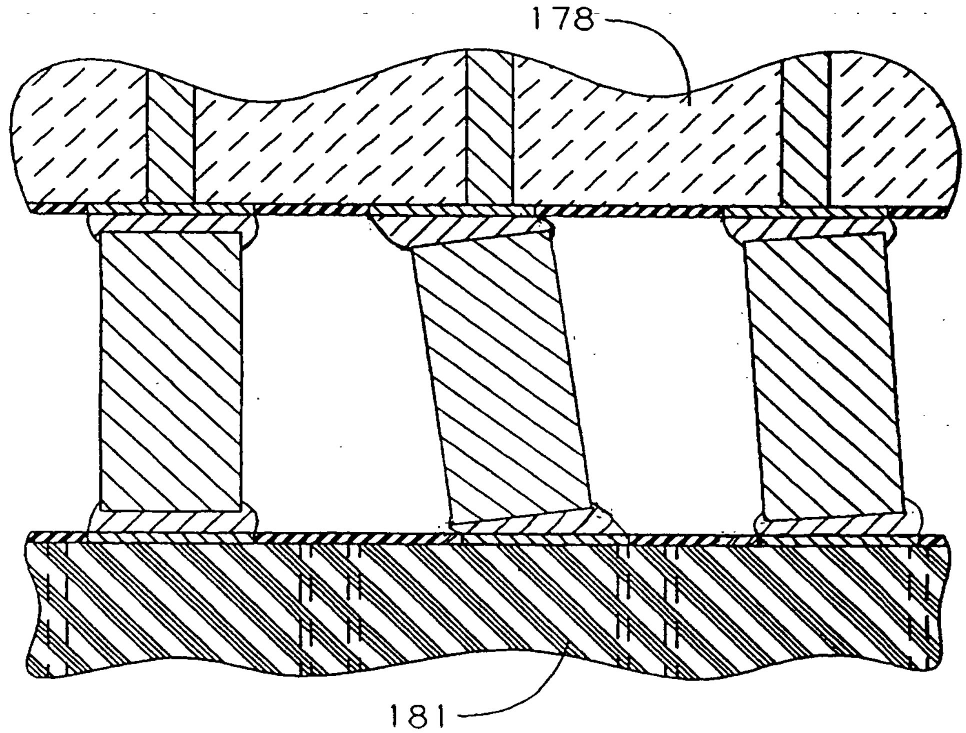


FIG. 19

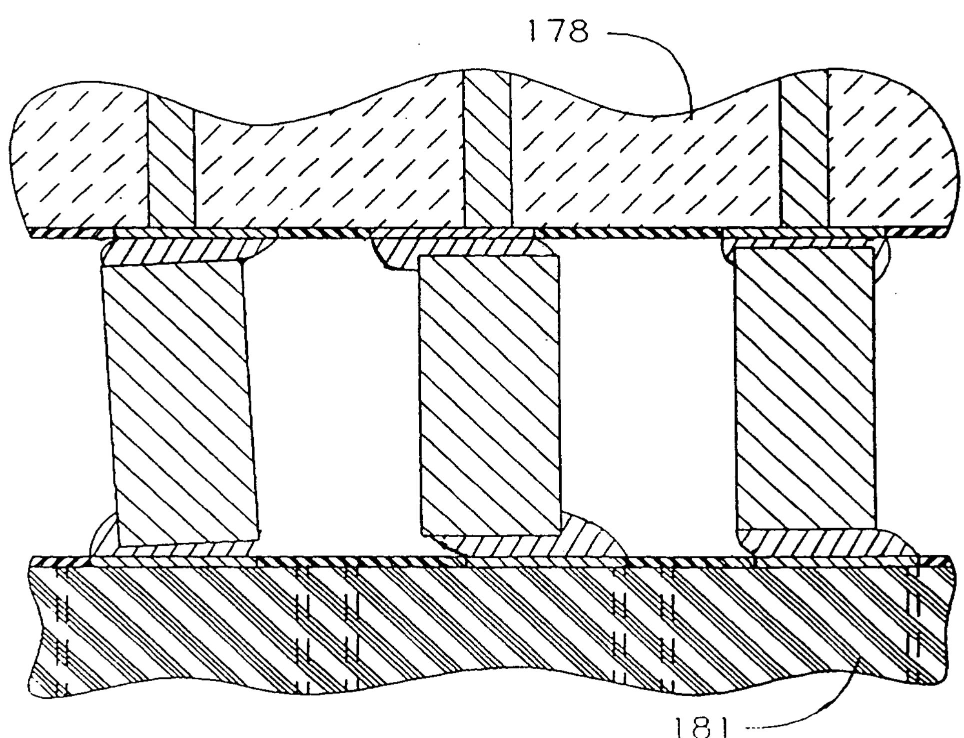


FIG. 18

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Office européen des brevets

(11) EP 0 650 795 A3

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(54) **Solder ball connections and assembly process**

(57) High melting temperature Pb/Sn 95/5 solder balls (18) are connected to copper pads on the bottom of a ceramic chip carrier substrate (10) by low melting temperature eutectic Pb/Sn solder. The connection is made by quick reflow to prevent dissolving Pb into the eutectic solder and raising its melting temperature. Then the module is placed on a fiberglass-epoxy circuit board with the solder balls on eutectic Pb/Sn solder bumps on copper pads of the board. The structure is reflowed to simultaneously melt the solder on both sides of the balls to allow each ball to center between the carrier pad and circuit board pad to form a more symmetric joint. This process results in structure that are more reliable under high temperature cycling. Also, to further improve reliability, the balls are made as large as the I/O spacing allows without bridging beam on balls; the two pads are about the same size with more solder on the smaller pad; the pads are at least 75% of the ball diameter; and the eutectic joints are made as large as possible without bridging between pads. For reliability at even higher temperature cycles or larger substrate sizes columns are used instead of balls.

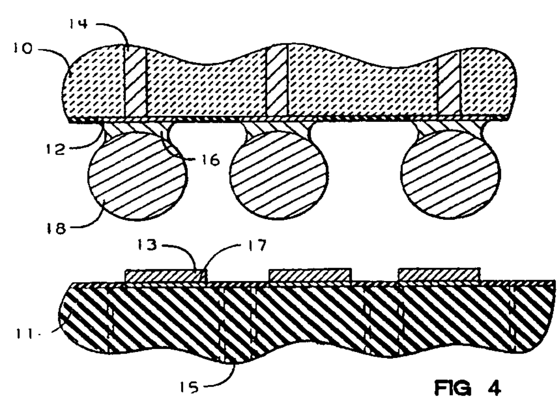

FIG 4

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EUROPEAN SEARCH REPORT

Application Number
EP 94 11 4605

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-5 060 844 (BEHUN ET AL.) * column 3, last paragraph - column 4, line 38; figures 1A-3 * ---	1,4,6, 10,11, 18,19, 22,23, 29-31	B23K1/00 H05K3/34
X,D	US-A-5 147 084 (BEHUN ET AL) * the whole document * ---	1,4,6, 10,11, 18,19, 22,23, 29-31	
A,D	ELECTRONIC ENGINEERING TIMES, 15 March 1993, pages 37,-47-50, DERMAN: "Solder balls make connections" * the whole document * ---	9,13,14	
A	EP-A-0 084 464 (NORTH AMERICAN SPECIALITIES CORP.) * claims 1-7; figure 2 * ---	1-31	TECHNICAL FIELDS SEARCHED (Int.Cl.6) B23K H05K
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 29, no. 4, ARMONK, NEW JERSEY, USA, page 1646 "Copper ball standoff for surface-mounted attachment of mlc substrates on laminates." * the whole document * -----	1-31	

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 April 1996	HERBRETEAU, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.

namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: 1-31

European Patent Office

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-31 Process for producing an interconnect assembly
2. Claims: 32-45 Information handling system